



UVM VIP-TSC Status

Co-Chair – Hillel Miller (Freescale)

Co-Chair – Thomas Alsop (Intel)

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Discussion Items

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Industry Need

- Verification solutions are ubiquitous and differ from company to company and within organizations in companies.
- The result is many different methods of doing the same thing, some methods being better than others, but all requiring retraining and expensive conversion costs.
- Best known methods are not always shared resulting in flawed and expensive to repair designs.
- Verification cannot easily package a solution to another external or internal user or design team.
- Validation engineering turn-around is high leading to expensive training overhead.



Why Standardization is Needed

- Verification Intellectual Property (VIP) in the industry is growing exponentially.
- We are seeing more companies which are completely SoC or moving in this direction. IP-Reuse is becoming a requirement.
 - This requires more sharing of VIP not only internally, but externally.
- Sharing VIP internally and externally requires interoperability of components.
 - Else, huge amounts of time and resources are consumed converting one form of VIP to another and in training on different methods used to create and use the VIP i.e. Major \$\$\$ lost!!
- IEEE 1800 spec (SystemVerilog) is becoming the next language of choice for design and validation. It's standardized but there is still no standard for using its VIP.



Our Mission

- Definition of standard technology and/or methods for realizing a modular, scalable, and re-usable generic verification environment targeted for all design abstraction levels RTL and above, which facilitates
 - Plug-n-play verification IP (vIP) reuse
 - Seamless VIP reuse independent of any vendor platform or methodology.
 - Interoperability between all vendor and user methodologies and company VIP allowing for a standard convergence path.
 - Promotes horizontal reuse (from one group to another group in one organization)
 - To a lesser extent, promotes vertical reuse (from unit → cluster → full-chip → system)



Committee Structure

- **Structure:**
 - Co-Chair: Hillel Miller (Freescale)
 - Co-Chair: Thomas Alsop (Intel)
 - Secretary: Adam Sherer (Cadence)
 - A large number of major users and EDA vendors are expected to actively participate in this committee



Membership

- These companies finalized this proposal
 - Intel
 - Freescale
 - Cadence
 - Mentor
 - Synopsys
 - Paradigm works
 - Verilab
 - Denali
 - Xilinx
 - Qualcomm
 - ST
 - Nokia
 - Sun
 - Texas Instrument
 - Springsoft
 - IBM
 - Aldec
- We fully expect broader participation



Major Deliverables

Milestone	Date	Result	Key Points
OVM/VMM Interoperability	July 2009	Best Practices Document and Library for doing interoperability between OVM and VMM	<ul style="list-style-type: none"> •Simulators supporting multiple base classes. •First joint library development on an Accellera TSC. •Strong team (Collaboration, Speed, Quality, Best in Industry).
UVM 1.0 EA	May 2010	User & Reference Guide, SV Library.	<ul style="list-style-type: none"> •Starting point OVM 2.1.1. •Key features: callbacks, end-of-test and message catching. •Documentation type selection. •Development process. •Project planning and execution. •UVM/VMM interoperability library used for transitioning.
UVM 1.0	October 2010 (planned)	User & Reference Guide, SV Library.	<ul style="list-style-type: none"> •Registers, Phasing and TLM. •Numerous other features. •We will be starting from this version. Infrastructure is being developed using the UVM 1.0 EA version.



UVM 1.0EA

- Released May 17th, 2010 !!!
- Two months of process development and agreement
 - Accellera has never done a software dev process (17 companies involved). Had to get this right. Looked at many solutions.
 - We wanted the process to scale with increased participation
 - Had to agree on requirements gathering process, spec creation, implementation flows, testing and overall voting processes.
 - Had to agree on practical considerations and logistics
- Release contains
 - All OVM 2.1.1 features (base-line for UVM)
 - Callback enhancements
 - End of test enhancements
 - Message/Report Catching
 - Reference Guide and Users Guide



UVM 1.0

- Will use UVM 1.0EA as starting point
- Potential substantial features for 2010:
 - Registers/Memory
 - TLM 2.0
 - Phasing extensions
- Miscellaneous feature improvements.
- Timeline will be feature driven, not schedule
 - Once feature set is agreed upon, pragmatic timeline will follow
- Process:
 - Documentation: Interoperability and Reference.
 - UVM library releases with development process.



Practical Considerations

- Requirements-gathering is underway
 - Key features from OVM will be maintained
 - TSC agreed to consider *complementary* functionality as additions to the baseline
 - Key guidelines:
 - Compatibility with existing OVM users as much as possible.
 - Enable VMM users with interoperability library as much as possible.
- A true IEEE standard spec should be created from the requirements, much like the 1800 spec.
- Development will be handled by members of the TSC. All members to approve requirements, feature specifications, implementation, testing and final document
- The joint effort will result in a true “universal” methodology standard. The TSC has approved the name “UVM” for “Universal Verification Methodology.”
- EDA vendors may provide their own (possibly open-source) compliant implementation of the standard
 - Whether or not the TSC releases a “reference” implementation
- Tar-ball released on the Accellera site.
- Development done on Source forge.



Logistics

- Membership
 - Only Accellera member companies are eligible to vote
 - Committee will encourage non-Accellera participants to join Accellera
- Balloting
 - The TC will turn the Accellera standard over to the IEEE for a full balloting process per the timeline if BoD approves
- Will follow Accellera Operational Rules
- Requirements and specification process as proposed by Jay Lawrence (See documents).
- Development and implementation process as proposed by Tom Alsop and Ambar Sakar (See documents).
- Source forge guidelines for SW control management as proposed by Ambar Sakar (see document).
- Bug submission and tracking as proposed by Tom Alsop (see document).



Schedule – Tentative → Feature driven

Top 10 features for UVM 1.0	March 14, 2010
Requirements for UVM 1.0 EA	March 25, 2010
Specification for UVM 1.0 EA	March 30, 2010
All Code Entered	March 30, 2010
Release UVM 1.0 EA	May 14, 2010
Requirements UVM 1.0	Aug 7, 2010
Specification UVM 1.0	Aug 30, 2010
Implementation & Testing UVM 1.0	Sep 30, 2010
Documentation for UVM 1.0	Oct 7, 2010
Release UVM 1.0	Oct 30, 2010



UVM World

- Get the latest news/commentary on UVM World
<http://www.uvmworld.org/>
- Forums & Threads
 - When is UVM 1.0 going to be released?
 - How do I file bugs, request enhancements to UVM?
 - Start your own thread, ask a question, share your knowledge, etc...
- Pointer to the Accellera download of UVM 1.0EA
- Pointer to UVM Mantis for bugs and enhancements reporting.



Summary

- There is a very clear need for a standardization of verification IP.
- End users both across company and industry boundaries will benefit tremendously.
- Collaboration, IP-Reuse, and sharing of IP will be enabled across the industry.
- Time to market and product cost will decrease for all companies using these solutions thereby benefiting the global market.
- UVM is making incredible progress!
- UVM is intended to standardize the industry on a single verification methodology!



Questions

