

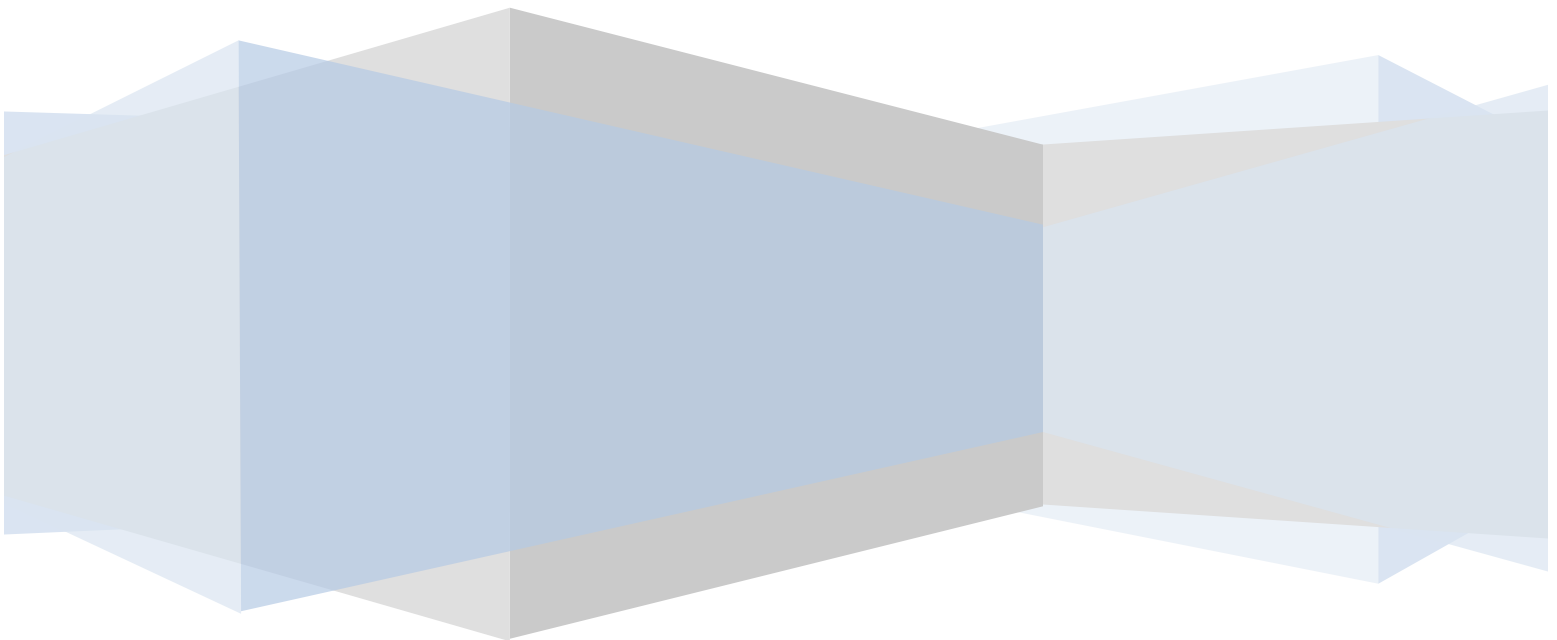
www.uvmworld.org



UVM Reference Flow 1.0

Overview and Capabilities

Contribution by Cadence Design Systems, Inc



OVERVIEW

The [Universal Verification Methodology \(UVM\) Reference Flow 1.0](#) is an open-source contribution by Cadence Design Systems, Inc. to the UVM community for purposes of:

- Providing a UVM reference for users to train and learn
- Enabling a uniform environment for executing UVM code
- Establishing a standardized solution for benchmarking
- Demonstrating the features provided with UVM Verification Components (UVCs)

It is the intention of Cadence to update the UVM Reference Flow synchronous with each UVM base class library change, with the version number being consistent for ease of understanding. Users are encouraged to contribute additional code, design IP, verification IP or documentation.

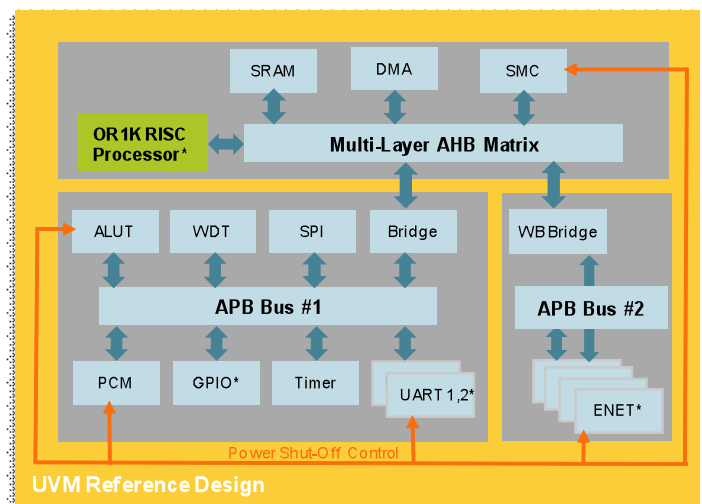
DESIGN & VERIFICATION ENVIRONMENT

DESIGN

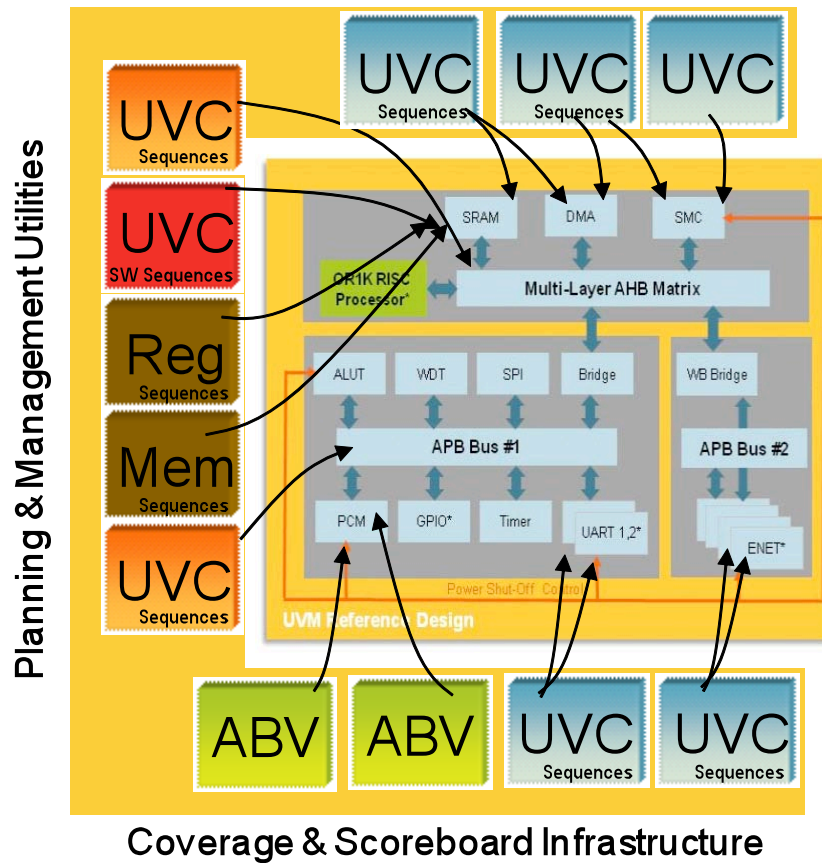
The UVM Reference Flow 1.0 design is an OpenCores RISC-based SOC design. The design (see diagram) consists of multiple interconnecting subsections. The three interconnecting bus systems include a multi-layer AHB bus, two APB buses and a wishbone bus for connecting both the processor and the Ethernet controllers. There are low-power sections of the design for power shut off, controlled by the power control module block (PCM).

VERIFICATION ENVIRONMENT

The UVM Reference Flow 1.0 verification environment consists of six different UVM Verification Components (UVC). The purpose of the UVCs is to provide stimulus to interfaces on the design for purposes of measuring functional coverage. See the table further on in this document for a list of the verification components provided. The SystemVerilog UVCs provided use standard IEEE1800 SystemVerilog constructs, enabling execution in any IEEE1800-compliant simulator. Users can also implement low-power verification techniques using the Common Power Format (CPF) or Unified Power Format (UPF). Future enhancements to the verification environment will include device drivers, verification components written in native Specman / e, and additional UVCs, such as for the Ethernet MAC controller.



Virtual Sequence Generation



USER BENEFITS

- Pipe-cleaning advanced verification flows
 - Allow feasibility study on a shareable test case
 - Decouple complexity of flows and complexity of designs
 - Deployment of verification methodologies
- Standard tools and methods ramp-up
 - Using a common design has major benefit on training efficiency
 - Customer tools integrated into a standardized flow
- Easily demonstrating interoperability
 - Open source is key to prove interoperability across tools

LICENSING AND PACKAGING

All of the components within the design and verification environment are open source, however users should be aware of the combination of [Apache 2.0](#) and GNU licenses used within this reference flow. The combination of the two licenses is required for the design components, where there are four design IP blocks that use the GNU Lesser General Public License (LGPL) Version 3. These blocks are the RISC processor OR1K, the Ethernet Controller, the UART and the SPI block. All four of these blocks come from the OpenCores website and can be found at www.opencores.org. All license text is included in the download file. For user convenience, Cadence has assembled all components, which use the UVM 1.0 base class libraries, into a single tar file for users to download. A UVM Reference Flow User Guide is included to aid users in understanding how to use the environment. The download file includes the following design and verification components:

UVM Reference Flow 1.0 – Design IP

| Block | OpenCores IP | | Description | UVM Reference Flow - Design IP | | | |
|-------|----------------|------|--------------------------------|--------------------------------|--------|------------|----------|
| | Name | Type | | Design IP | Format | License | Bus I/F |
| 1 | OR1K Processor | HW | OpenCores OR1K RISC Processor | Verilog | Source | LGPL 3.0 | Wishbone |
| 2 | Ethernet MAC | HW | OpenCores 10/100 Ethernet MAC | Verilog | Source | LGPL 3.0 | Wishbone |
| 3 | RAM | HW | RAM Memory Models | Verilog Model | Source | Apache 2.0 | AHB |
| 4 | DMA | HW | Direct Memory Access | Verilog | Source | Apache 2.0 | AHB |
| 5 | ML AHB | HW | AMBA Multi-layer AHB Bus | Verilog | Source | Apache 2.0 | AHB |
| 6 | AHB2APB | HW | AMBA Bridge from AHB to APB | Verilog | Source | Apache 2.0 | AHB |
| 7 | WB2AHB | HW | Wishbone to AMBA AHB bridge | Verilog | Source | Apache 2.0 | AHB |
| 8 | SPI | HW | Serial Peripheral Interface | Verilog | Source | LGPL 3.0 | APB |
| 9 | UART | HW | OpenCores Serial Bus Interface | Verilog | Source | LGPL 3.0 | APB |
| 10 | GPIO | HW | OpenCores General Purpose IO | Verilog | Source | Apache 2.0 | APB |
| 11 | PCM | HW | Power Control Module | Verilog | Source | Apache 2.0 | APB |
| 12 | SMC | HW | Smart Memory Controller | Verilog | Source | Apache 2.0 | APB |
| 13 | TTC | HW | Timer Controller | Verilog | Source | Apache 2.0 | APB |
| 14 | ALUT | HW | Address Look Up Table | Verilog | Source | Apache 2.0 | APB |
| 15 | PADFRAME | HW | Pad frame | Verilog Model | Source | Apache 2.0 | - |
| 16 | LDO | HW | Linear DropOut Regulator | Verilog Model | Source | Apache 2.0 | - |
| 17 | VCO | HW | Voltage controlled oscillator | Verilog Model | Source | Apache 2.0 | - |

UVM Reference Flow 1.0 – Verification IP

| Block | Name | Type | Description | UVM Reference Flow - Verification IP | | | | |
|-------|---------|------|-----------------------------|--------------------------------------|--------|---------|--------|------------|
| | | | | Type | UVC_SV | UVC_e | Format | License |
| 1 | AHB Bus | SW | AMBA AHB Bus | UVC | Yes | Q4'2010 | Source | Apache 2.0 |
| 2 | APB Bus | SW | AMBA APB Bus | UVC | Yes | Q4'2010 | Source | Apache 2.0 |
| 3 | UART | SW | UART | UVC | Yes | Q4'2010 | Source | Apache 2.0 |
| 4 | GPIO | SW | General Purpose IO | UVC | Yes | Q4'2010 | Source | Apache 2.0 |
| 5 | SPI | SW | Serial Peripheral Interface | UVC | Yes | Q4'2010 | Source | Apache 2.0 |
| 6 | REG MEM | SW | Register Memory UVC | UVC | Yes | Q4'2010 | Source | Apache 2.0 |

FOR MORE INFORMATION

For more information or if you have comments and questions, please go to the forum on UVM World – www.uvmworld.org. Cadence Incisive users should be aware of the Incisive Verification Kit, which provides workshops, hands-on labs and how-to videos which are based on extensions to [UVM Reference Flow](#) content.