

Doulos Solutions Workshop:
Easier UVM - functional verification for mainstream designers

Wednesday June 8, 2011

12.00pm to 1.30pm

Room 24B, San Diego Convention Center

SUMMARY:

Easier UVM is an approach to using Accellera's UVM, the Universal Verification Methodology, for functional verification by mainstream hardware designers as opposed to power users with specialist verification skills.

In this workshop, John Aynsley CTO of Doulos will present simple examples to illustrate a set of guidelines for the use of the UVM class library for functional verification. The goal is to enable design engineers with experience in Verilog or VHDL to become productive in UVM by learning a small number of new coding idioms, selected to minimize the conceptual clutter they have to deal with. As users become fluent with this set of basic idioms, they can then branch out to embrace the full feature set of UVM as and when they need.

You can [find out more detail and register here](#) - attendees who pre-register before DAC will receive a free copy of the UVM Golden Reference Guide, the first edition of which will be published at DAC. Also [check out other Easier UVM collateral here](#).

Please note:

The web links for the last paragraph are sequentially:

<http://www.doulos.com/easierUVM>

http://www.doulos.com/knowhow/sysverilog/uvm/easier_uvm/