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Silicon to Software™

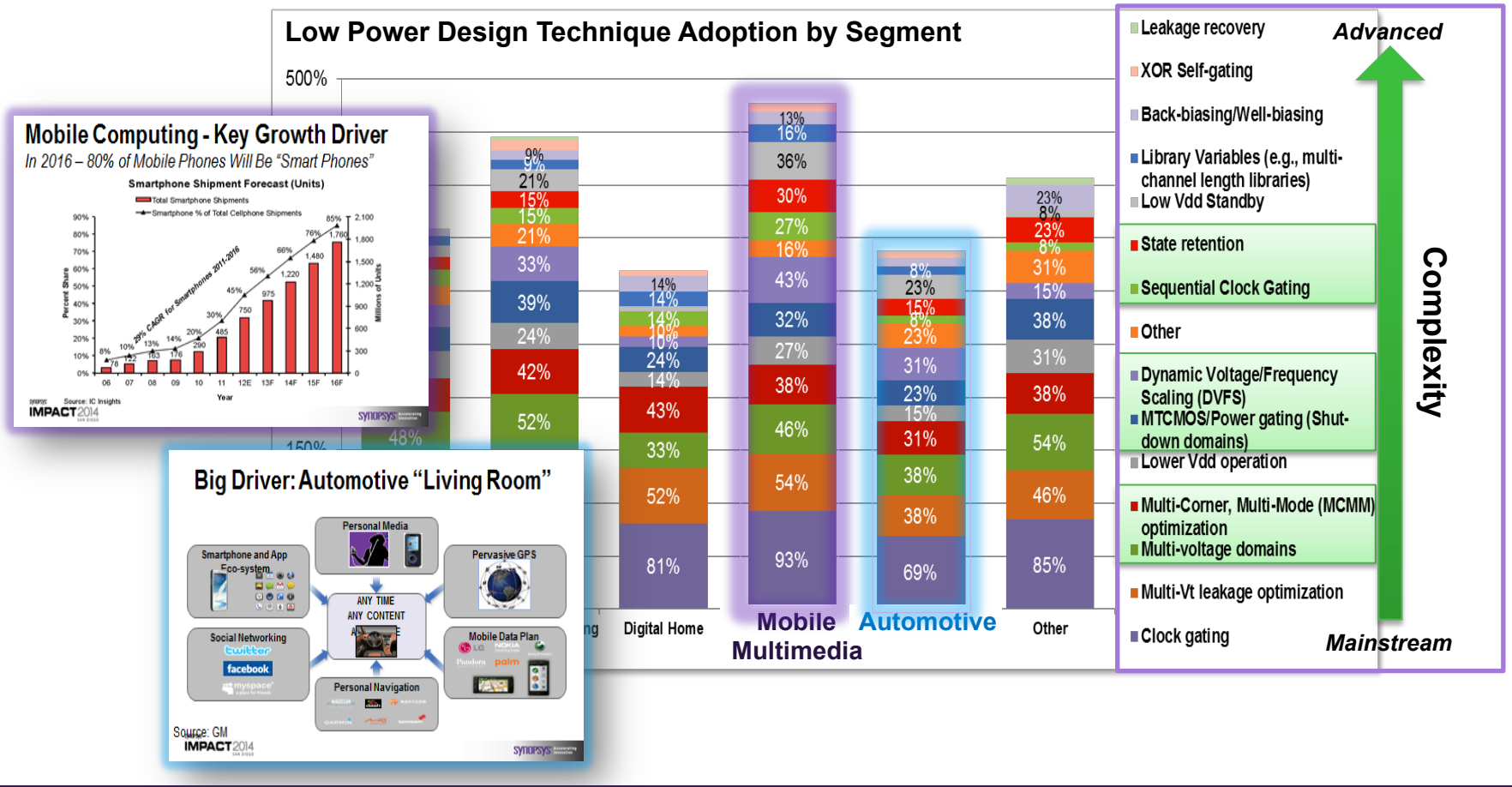
The ART of Power, Key to SoC Success

Introduction to Low Power Verification Methodology

Rich Chang

Product Marketing, Verification Group

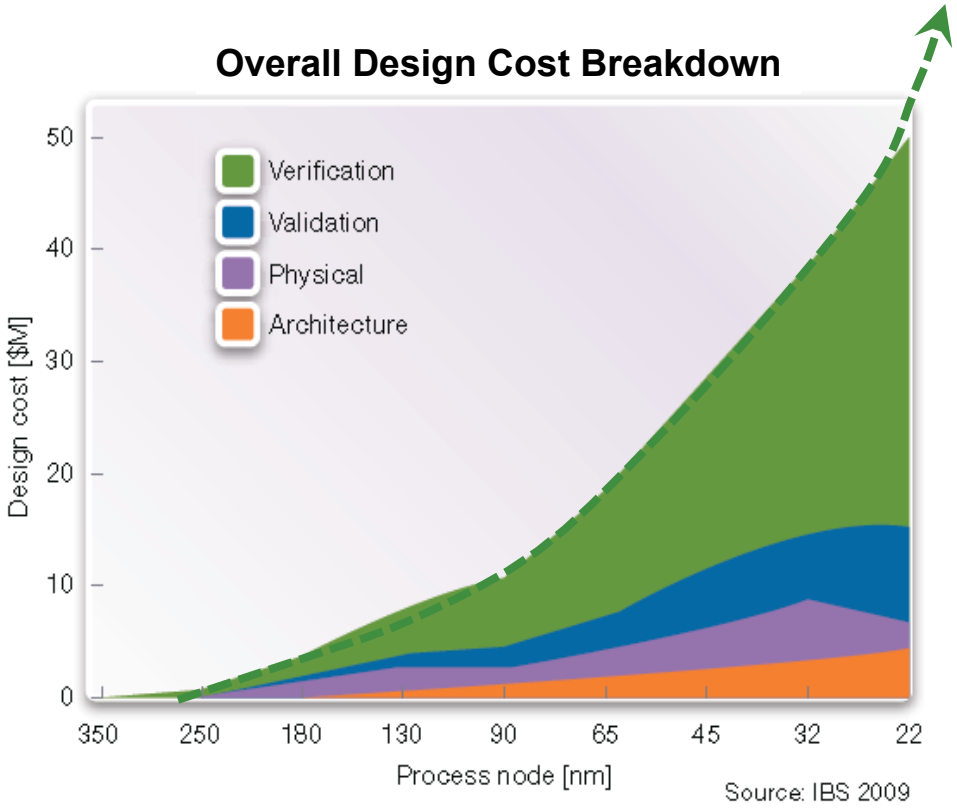
Low Power is Everywhere



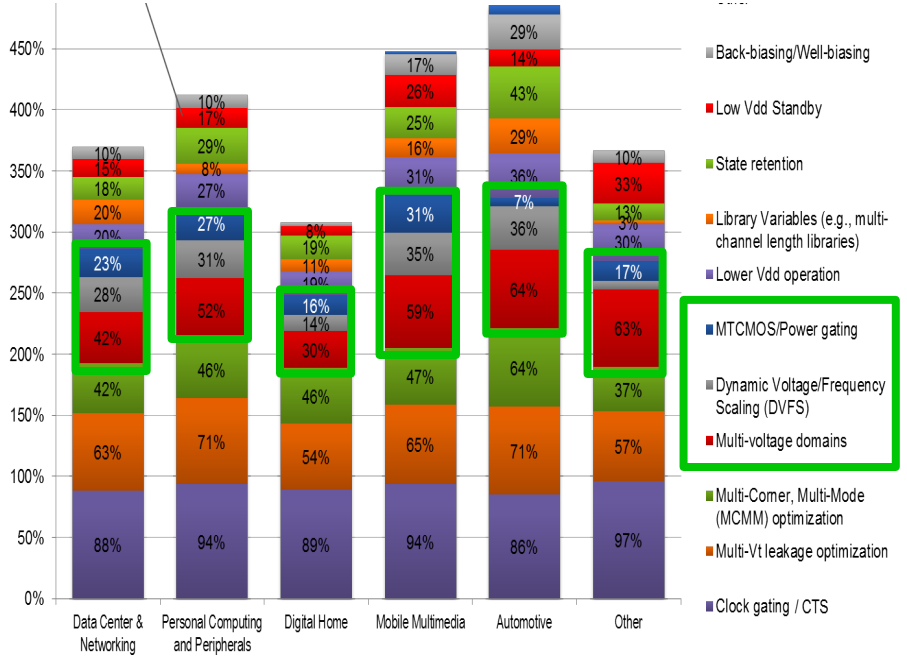
Mobile SoCs Driving Low Power Complexity Growth

Low Power Growth Driving Design Cost

Overall Design Cost Breakdown



LP Complexity Growing Across All Segments



Source: 2011-2012 Global SNUG surveys

Low power adoption causes increases in verification complexity

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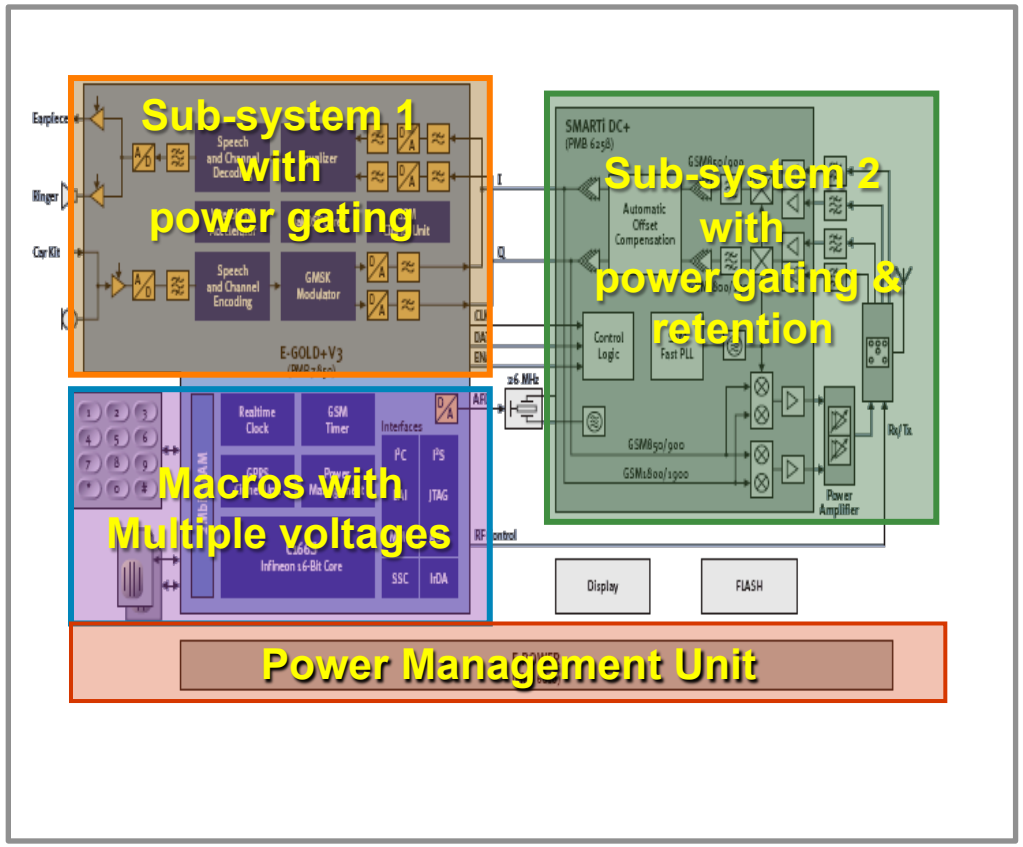
Low Power Verification Requirements

- Power intent validation
  - Requires static verification
  - Debug and simulation of LP states (shutdown, standby, retention..) and low power cells
- Coverage of new low power states at sub system level and SoC level
- Protocol checks for transitions in / out of low power states



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Functional Intent vs. Power Intent

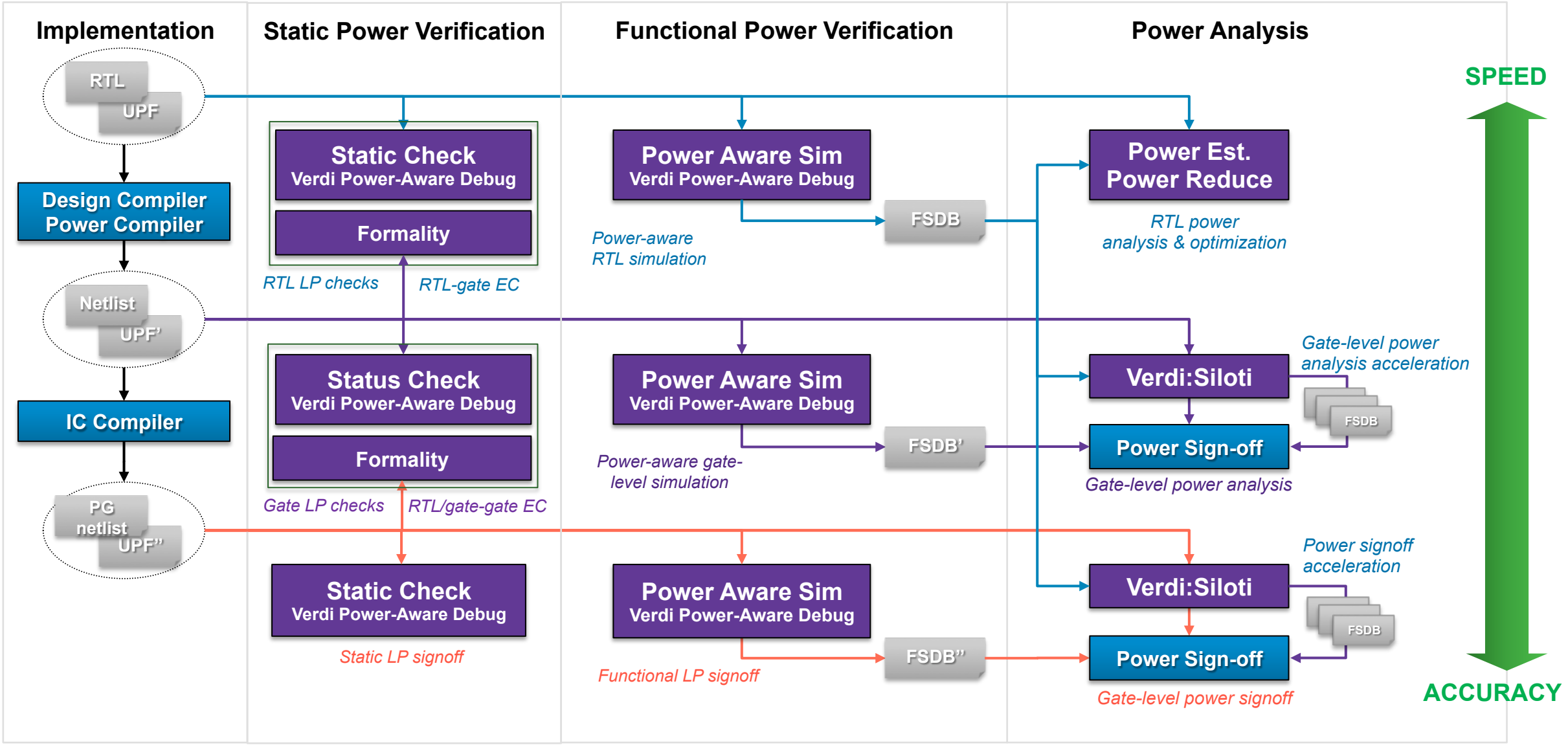
What is the difference?

Functional Intent	Power Intent

• **Architecture**
  • Design hierarchy
  • Data path
  • Custom blocks
• **Application**
  • State machines
  • Combinatorial logic
  • I/Os
  • EX: CPU, DSP, Cache
• **Usage of IP**
  • Industry-standard interfaces
  • Memories
  • etc
	• **Power distribution architecture**
	  • Power domains
	  • Supply rails
	  • Shutdown control
	• **Power strategy**
	  • Power state tables
	  • Operating voltages
	• **Usage of special cells**
	  • Isolation cells, Level shifters
	  • Power switches
	  • Retention registers

Captured in RTL	**Captured in UPF**

Synopsys Power Verification & Analysis Solutions



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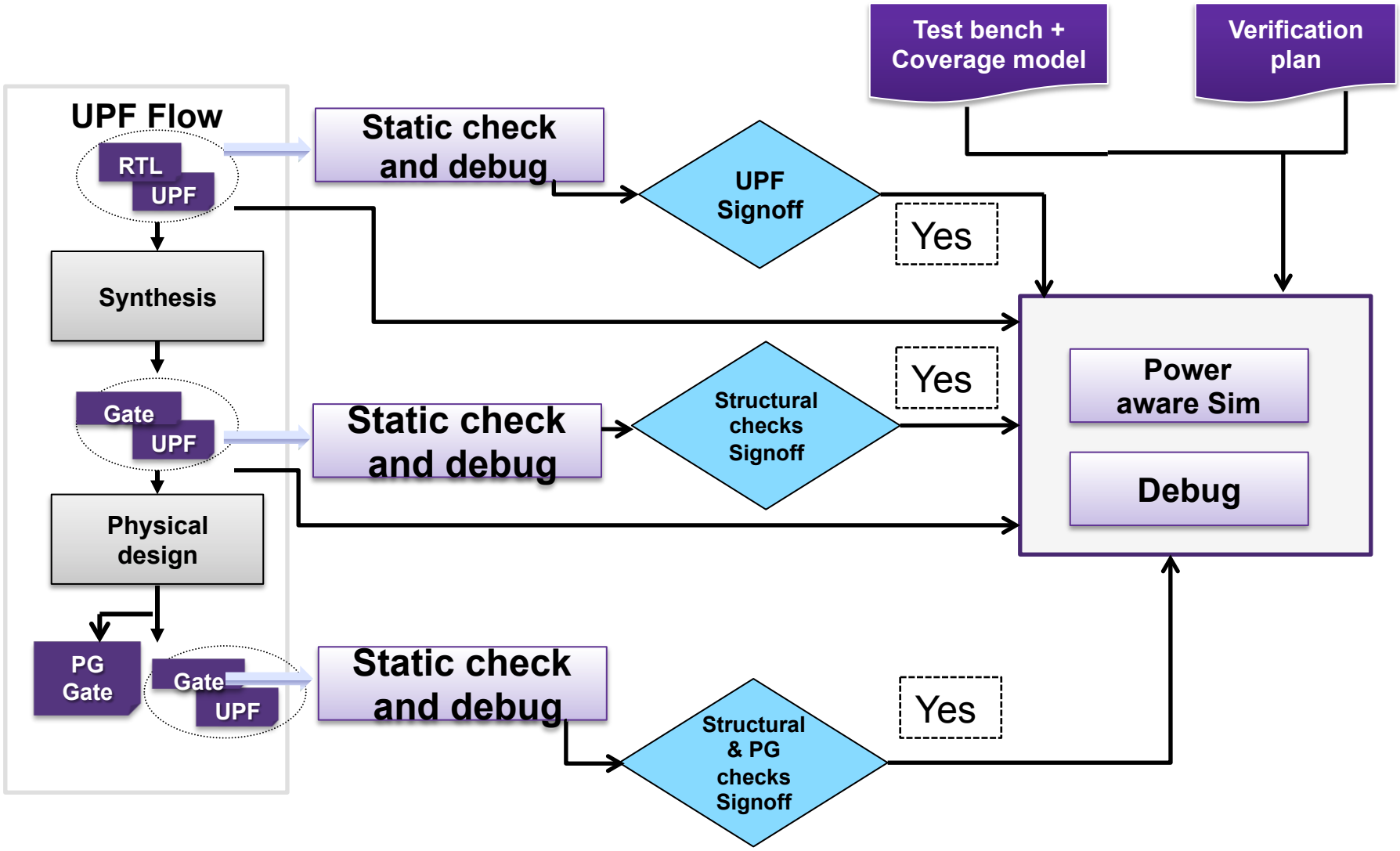
Complete and Efficient Static and Dynamic Verification



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Static Power Verification

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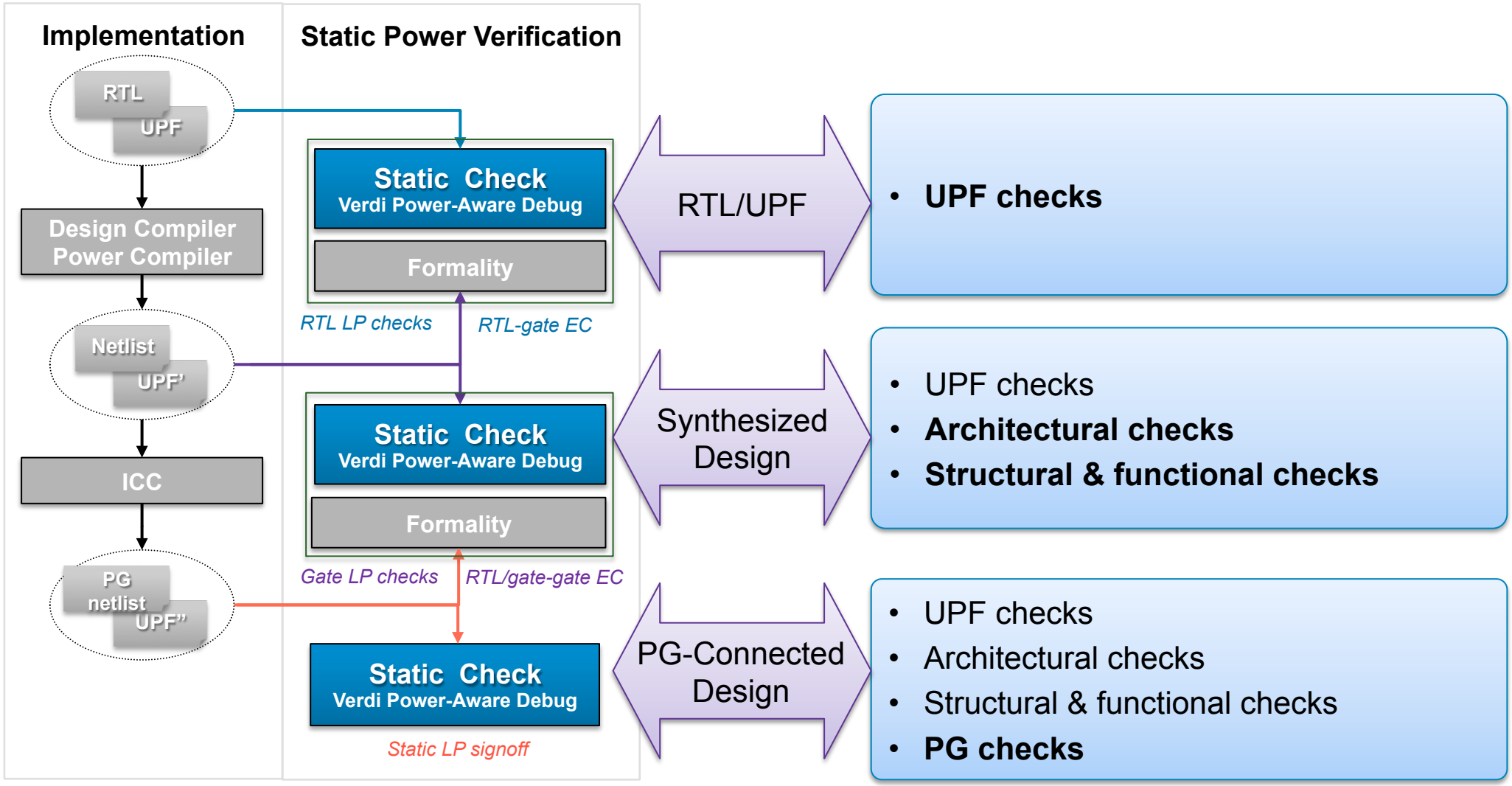
Synopsys Static Low Power Verification



Continually verify consistency between design intent and implementation

Static UPF Check

Next-Generation Low Power Static Checking and Signoff

Built from the ground-up for advanced SoCs

- Capacity and performance for full-chip verification
- Next-gen data model and engines

Consistency and correlation with implementation

- Design Compiler-like setup and use model
- Common format support: .lib, UPF, SDC, etc.
- Highly correlated hardware inference

Comprehensive set of applications

- Low Power, Formal+Apps, CDC, Rule Checking
- Unified UPF reading across applications

Efficient debug and root cause analysis

- Innovative LP-optimized error reporting and debugging

3-5X Performance and Capacity Advantage

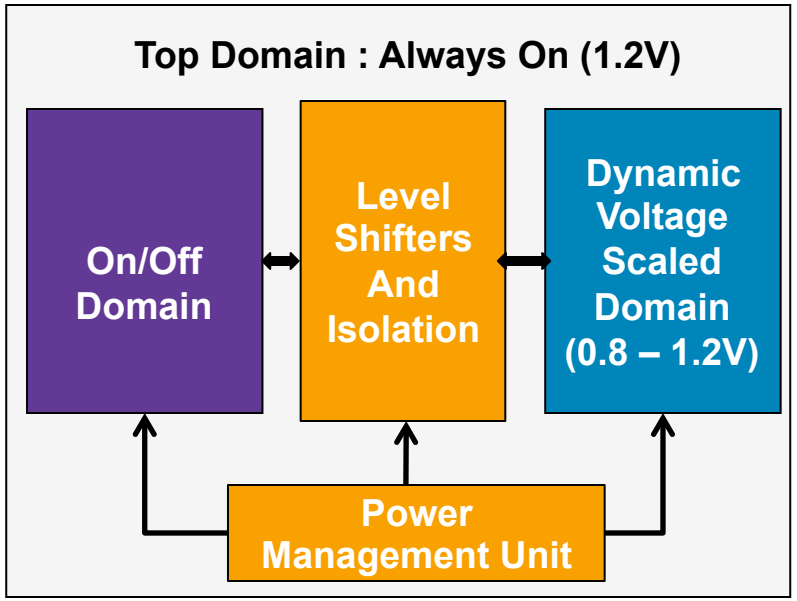
Static UPF Check

Features & Benefits

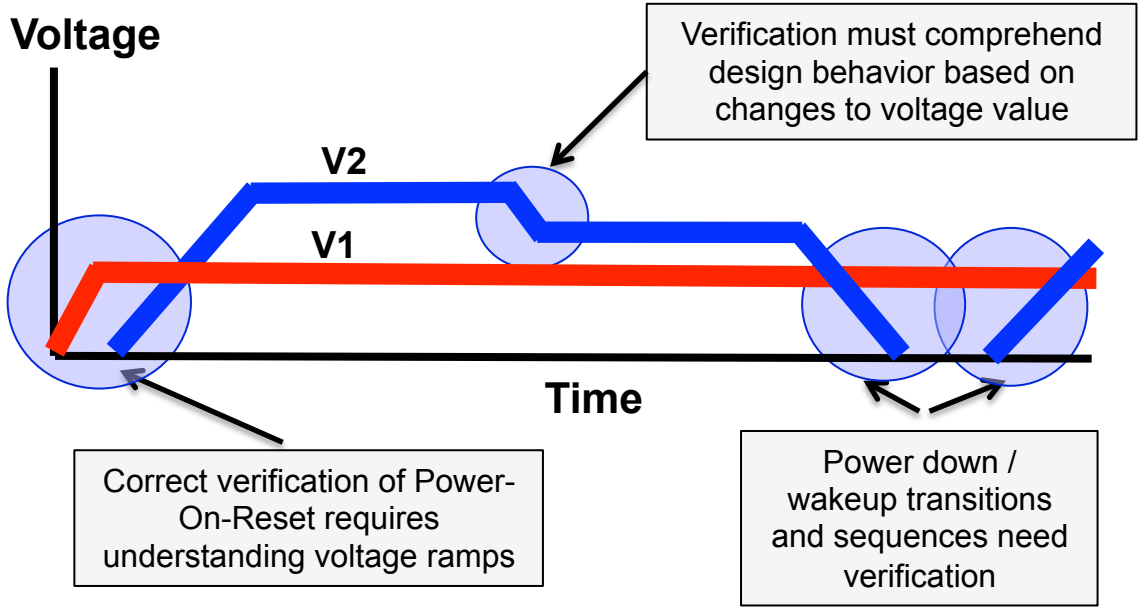
SoC-Scale Performance & Capacity	Loads full-chip SoCs at RTL and PG netlist—fast and complete checking through the entire design flow
DC TCL Support	Use DC setup for fast adoption; easily integrated into Synopsys implementation flows
Accurate Hardware Inference	Highest correlation of results between verification and implementation – Checks the right thing!
Production-Proven UPF Support	Best power network inference enables highest correlation to Synopsys low power implementation flows
Violation Noise Reduction Advanced LP Debug	Easiest and fastest violation prioritization, debug and root cause analysis

Dynamic Power Verification

Accurate Power-Aware Simulation



Design



Verification

VCS NLP's true multi-voltage simulation verifies designs at all operating voltages / transitions

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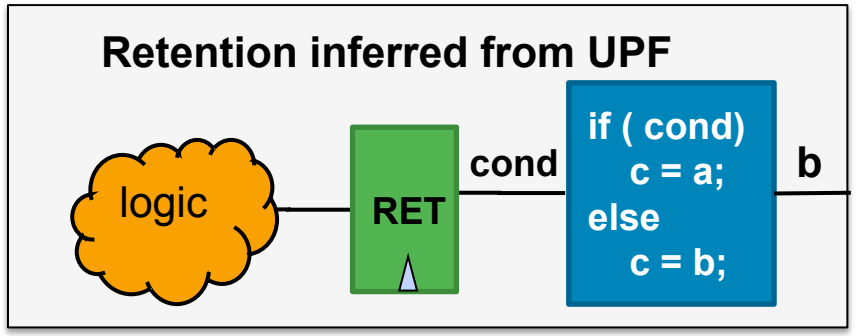
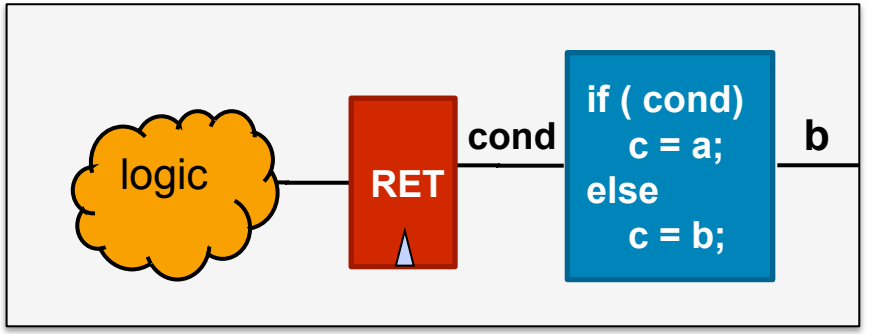
Accurate Power Aware Simulation

Native integration with advanced X-Prop catches X-optimism at RTL

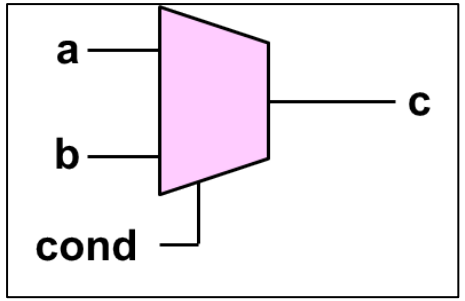
Intended Design After Restore



Actual Simulation After Restore



Circuit 1



cond	a	b	c(RTL)	c(HW)	c(GLS with circuit 1)	c(with XPROP tmerge)
x	0	0	0	0	0	0
x	0	1	1	0/1	x	x
x	1	0	0	0/1	x	x
x	1	1	1	1	1	1

X-optimism at RTL caught !!

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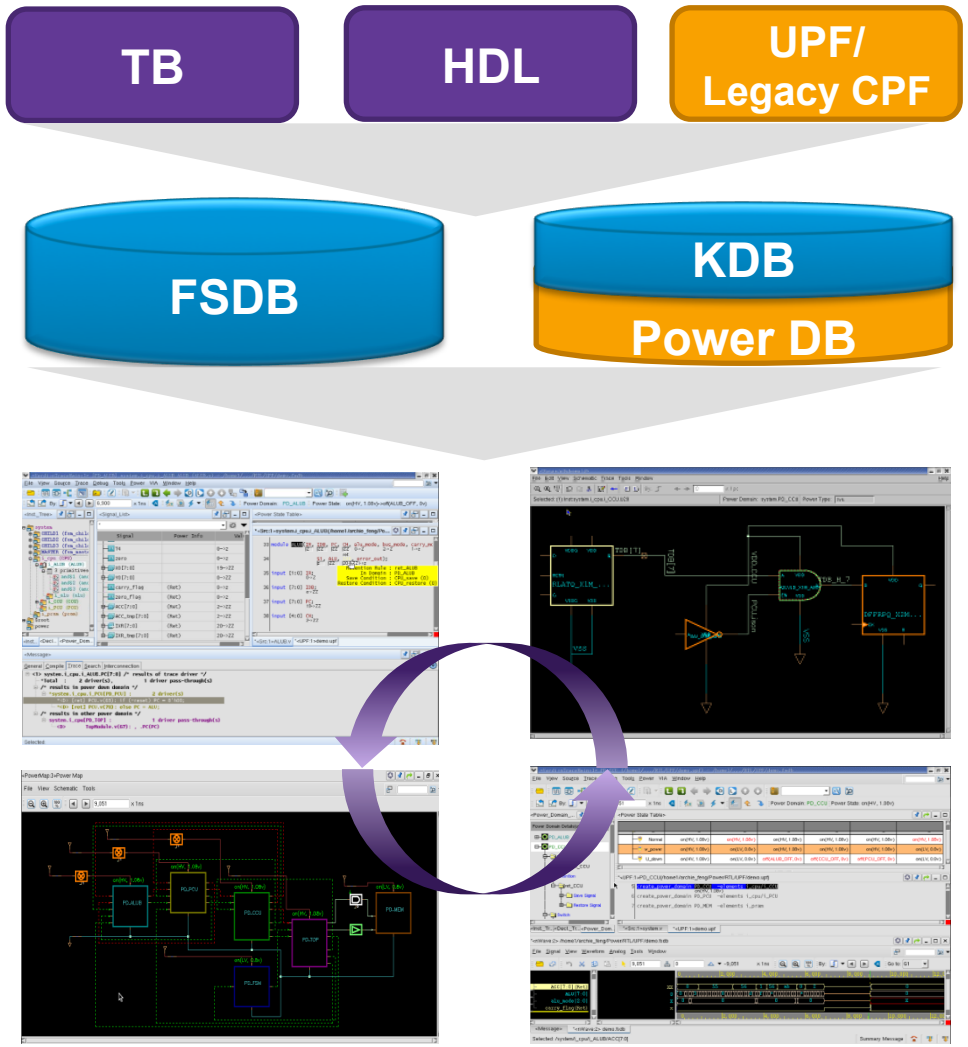
Power Aware Simulation

Benefits

Highest Accuracy	Catch corner case LP bugs with voltage-aware simulation and comprehensive support for all advanced LP techniques
High Performance	Enables broad use of LP simulation with the lowest impact on throughput and resources
Unified UPF Support	Common UPF support enables unified LP verification with excellent ease-of-use and correlation across simulation and debug flows
LP Assertions and Coverage	Full LP planning and coverage features, and automated LP assertions enable comprehensive coverage-driven verification methodologies
Advanced LP Debug	LP debug and coverage is natively integrated in Verdi, including power event visualization, powerful X-tracing, and cross-linking to UPF

Power-Aware Debug



Comprehensive Design Views

- Power-Aware Design Hierarchy
- Complete Schematic Views
- Annotated Power Intent

Power Intent Visualization

- Power Manager Browser
- Power Map
- Impacted Signal Report

Power-Aware Debug Automation

- Power-Aware Temporal Flow View
- Power Specific Waveform Debug
- Power Sequence Analysis

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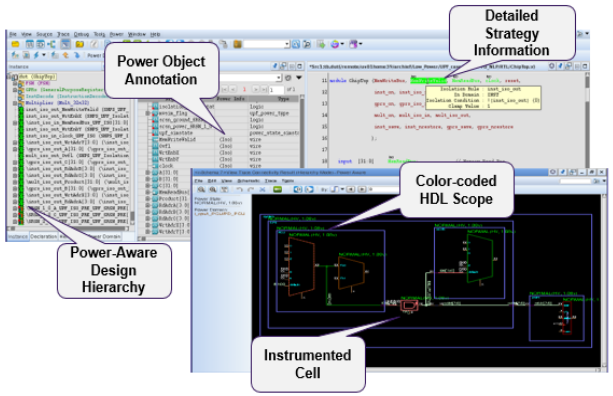
Power-Aware Debug Highlights

Comprehensive Design Views

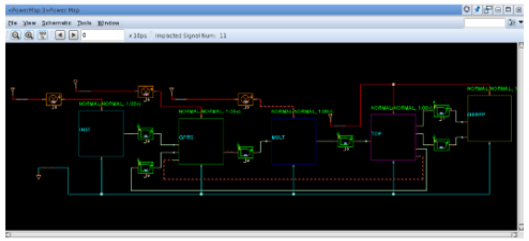
Including Design and Instrumented Power Objects



- Unified design and power management hierarchy
- Integrated schematic views include power objects
  - Isolation cells
  - Retention cells
  - Level-Shifters etc.
- Annotations provide relevant power intent information

Abstracted Power Domain View

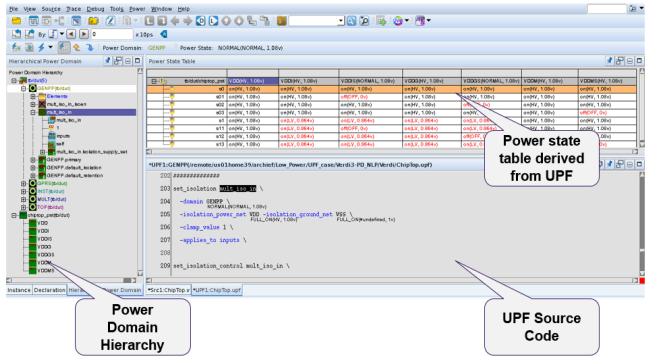
Power Map



- Topology of design based on power domain including:
  - Connectivity of power domains
  - Isolation/Retention/Level-Shifter/Repeater strategies
  - Power distribution network
  - Automatic highlighting of violations of isolation and level-shifter rules

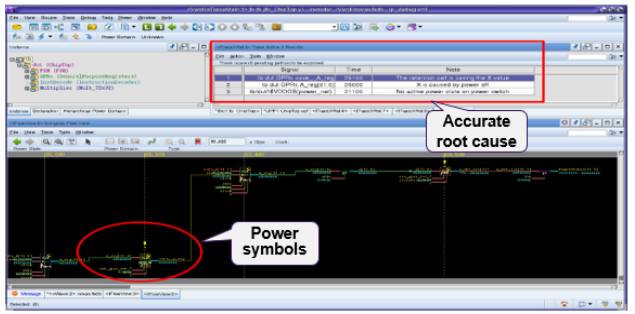
Dedicated Power Management Browser

Power Manager



- Power domain hierarchy including rules for
  - Isolation
  - Retention
  - Level-shift
  - Power switch
- UPF source code window for cross-reference
- Power state table derived from UPF for visualizing power mode transitions
  - Illegal state where mismatch occurred

Power-Aware Temporal Flow View



- Performs behavioral analysis on design, simulation AND power intent
- Automatically traces design behavior across multiple cycles
- Identifies root-cause taking instrumented cells and their values into consideration

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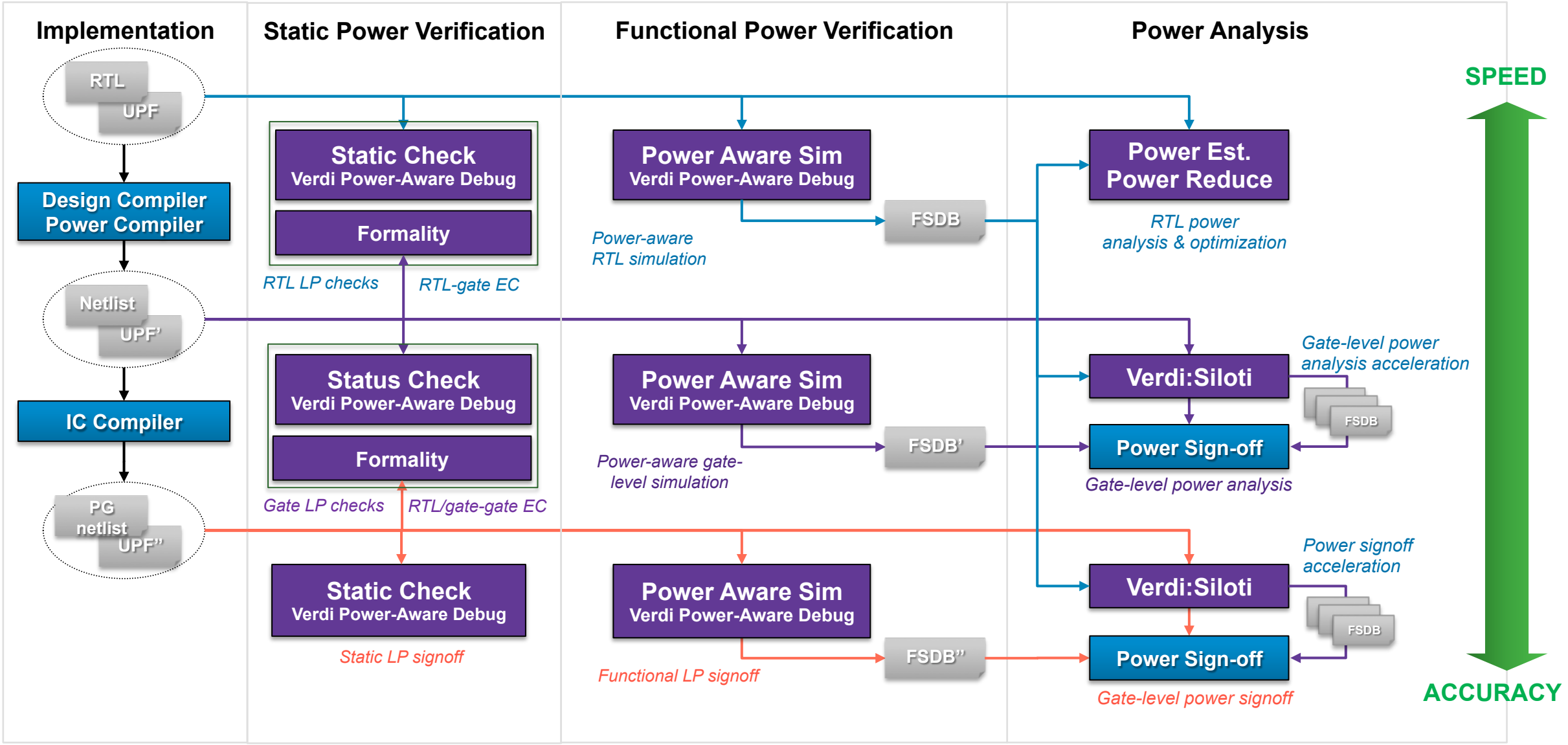
RTL Power Analysis & Optimization

Synopsys Power Verification & Analysis Solutions



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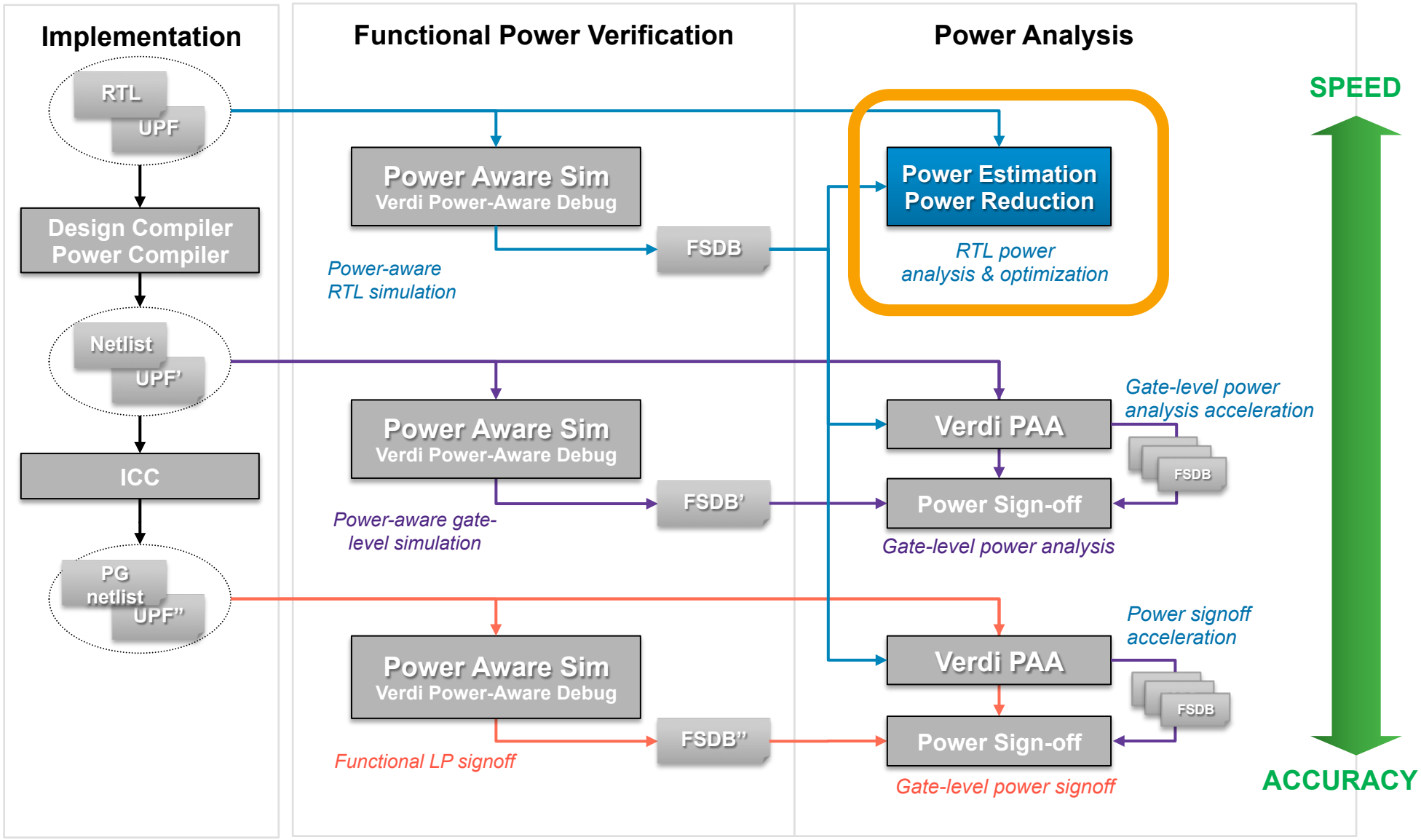
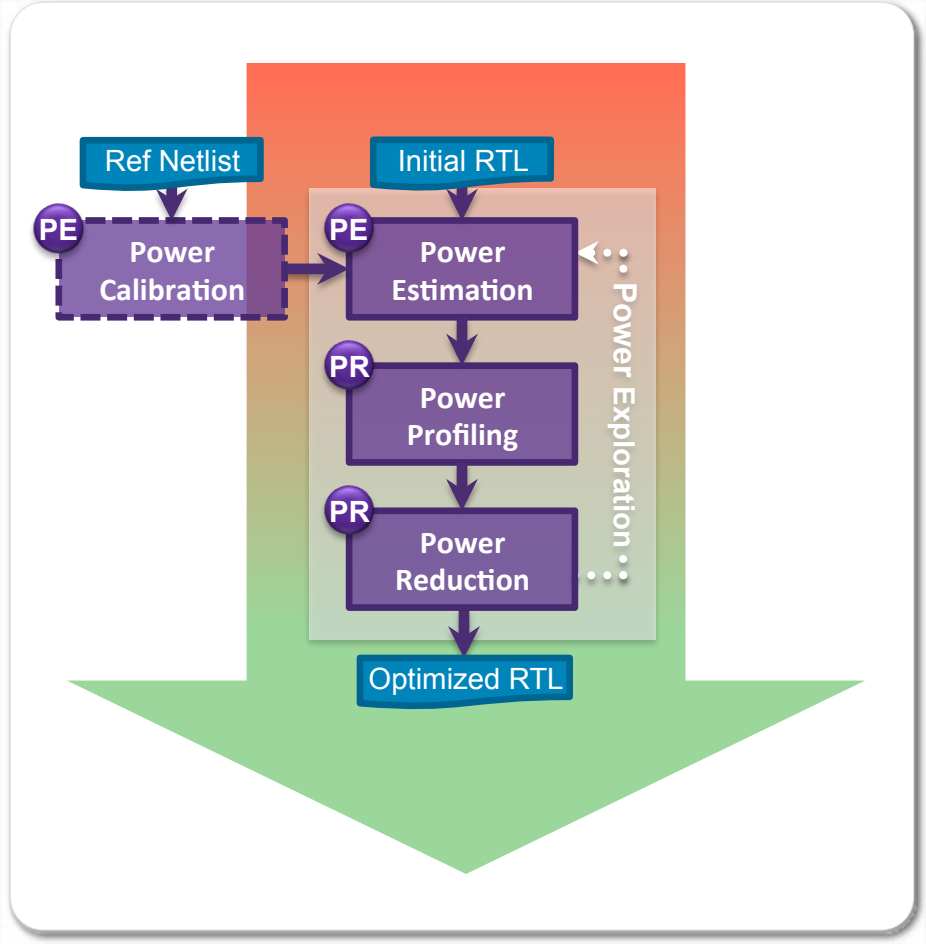
Synopsys Power Analysis Solutions



RTL Power Optimization Flow

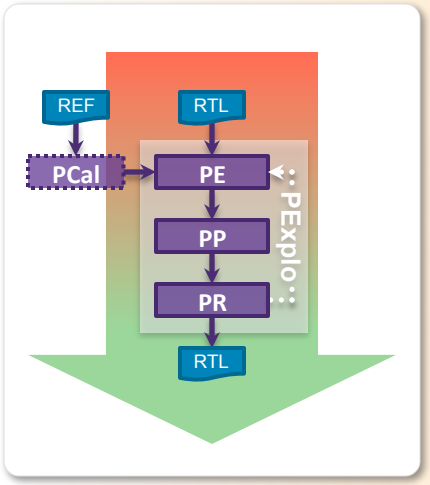


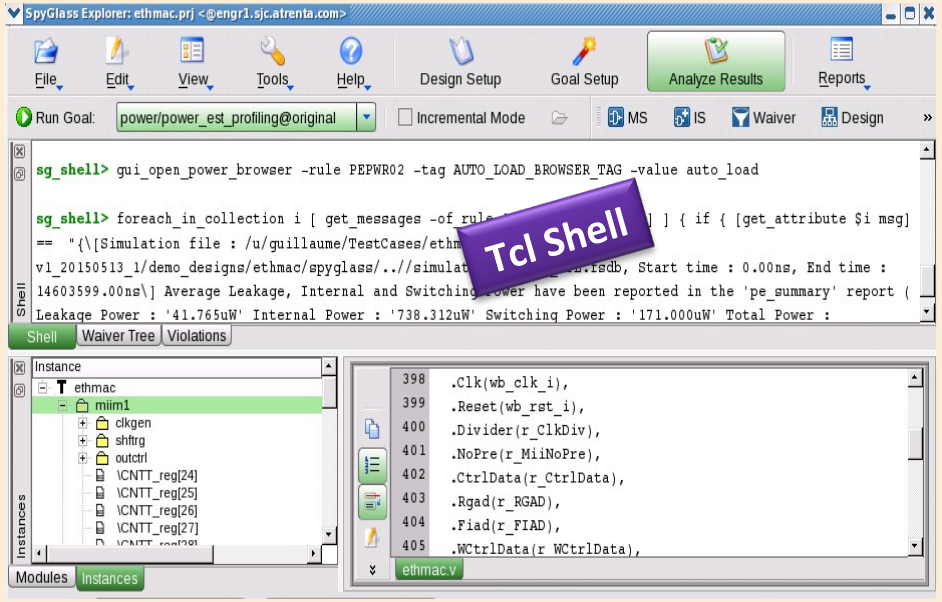
PE SpyGlass Power Estimate

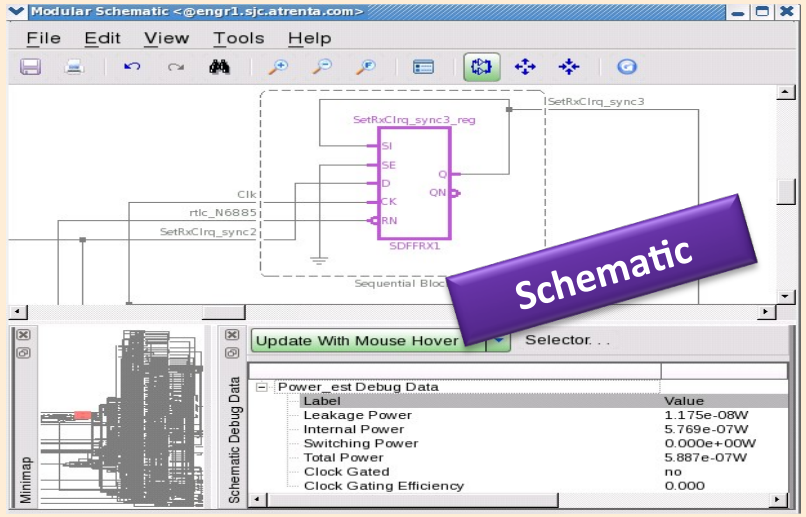
PR SpyGlass Power Reduce

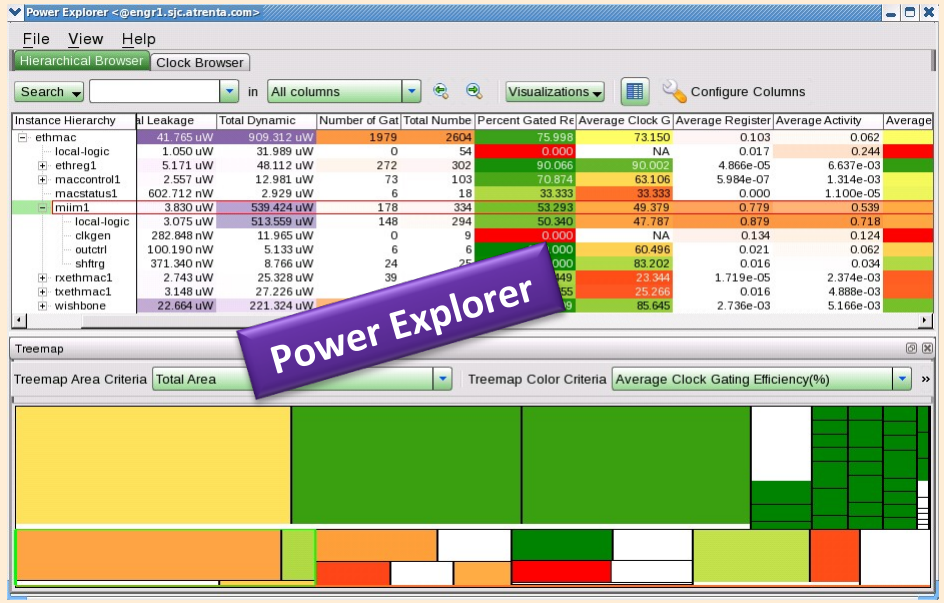
Optional

Designer View

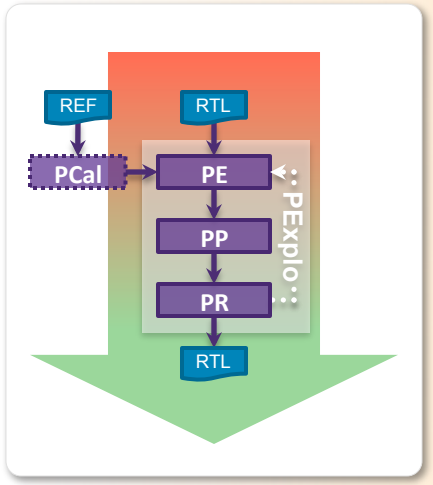








Summary View



Atrenta DashBoard - Spyglass Power Estimation/Reduction Report

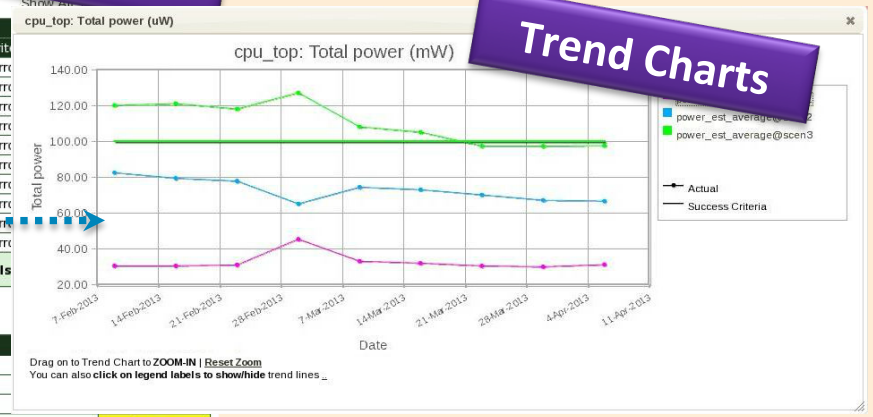
Pass / Fail Report

ethmac

Module: ethmac

Quality Goals	Run Completed At	Run Time	Run Status	Unresolved fatal	Unresolved error	Unresolved warning	Waived error	Waived warning	Success Crit
cdc_setup	N/A		Not started	0	0	0	0	0	Fatal =0, Err
power_est_average@original	05-20-2014 16:39:44	0:0:49 (49 secs)	Completed	0	0	9	0	0	Fatal =0, Err
cdc_verify_struct@original	N/A		Not started	0	0	0	0	0	Fatal =0, Err
power_profiling@original	05-20-2014 16:40:22	0:0:29 (29 secs)	Completed	0	1	9	0	0	Fatal =0, Err
power_guidance	05-20-2014 16:40:59	0:0:28 (28 secs)	Completed	0	0	13	0	0	Fatal =0, Err
power_mem_reduction	05-20-2014 16:44:12	0:2:59 (179 secs)	Completed	0	0	13	0	0	Fatal =0, Err
selective_autofix@RME_1	05-20-2014 16:45:00	0:0:40 (40 secs)	Completed	0	0	3	0	0	Fatal =0, Err
sec@RME_1	05-20-2014 16:45:33	0:0:23 (23 secs)	Completed	0	0	3	0	0	Fatal =0, Err
power_est_average@RME_1	N/A		Not started	0	0	0	0	0	Fatal =0, Err
power_profiling@RME_1	N/A		Not started	0	0	0	0	0	Fatal =0, Err
Summary			**Not completed**	**0**	**1**	**50**	**0**	**0**	**Failed goals**

Trend Charts



Category	Design Objective	Success Criteria	
Power	Internal power = 364.036uW	Not set	
	Leakage power = 40.370uW	Not set	
	Switching power = 195.229uW	Not set	
	Total power = 599.634uW	Not set	Ignore
Summary		**Failed objectives = 0**	

RTL Signoff Report

SPYGLASS DataSheet

Spyglass Power Estimation/Reduction
Created: Tue May 20 16:45:35 PDT 2014 by guillaume

Power (599.634uW total) Collapse

Technology	dti_sp_tm28hpmhvt_256x32_4ww1x_m_typ_lib, tsmc_130_typical
Register bit width threshold for clock gating	3
Registers enabled with clock gating	1963 (Total 2346)
Number of non gated registers	476
Clock Gating percentage	79.719%
Clock Gating efficiency	76.54%
Leakage Power	40.370uW
Internal Power	364.036uW
Switching Power	195.229uW
Total Power	599.634uW
Power Savings	2.061uW

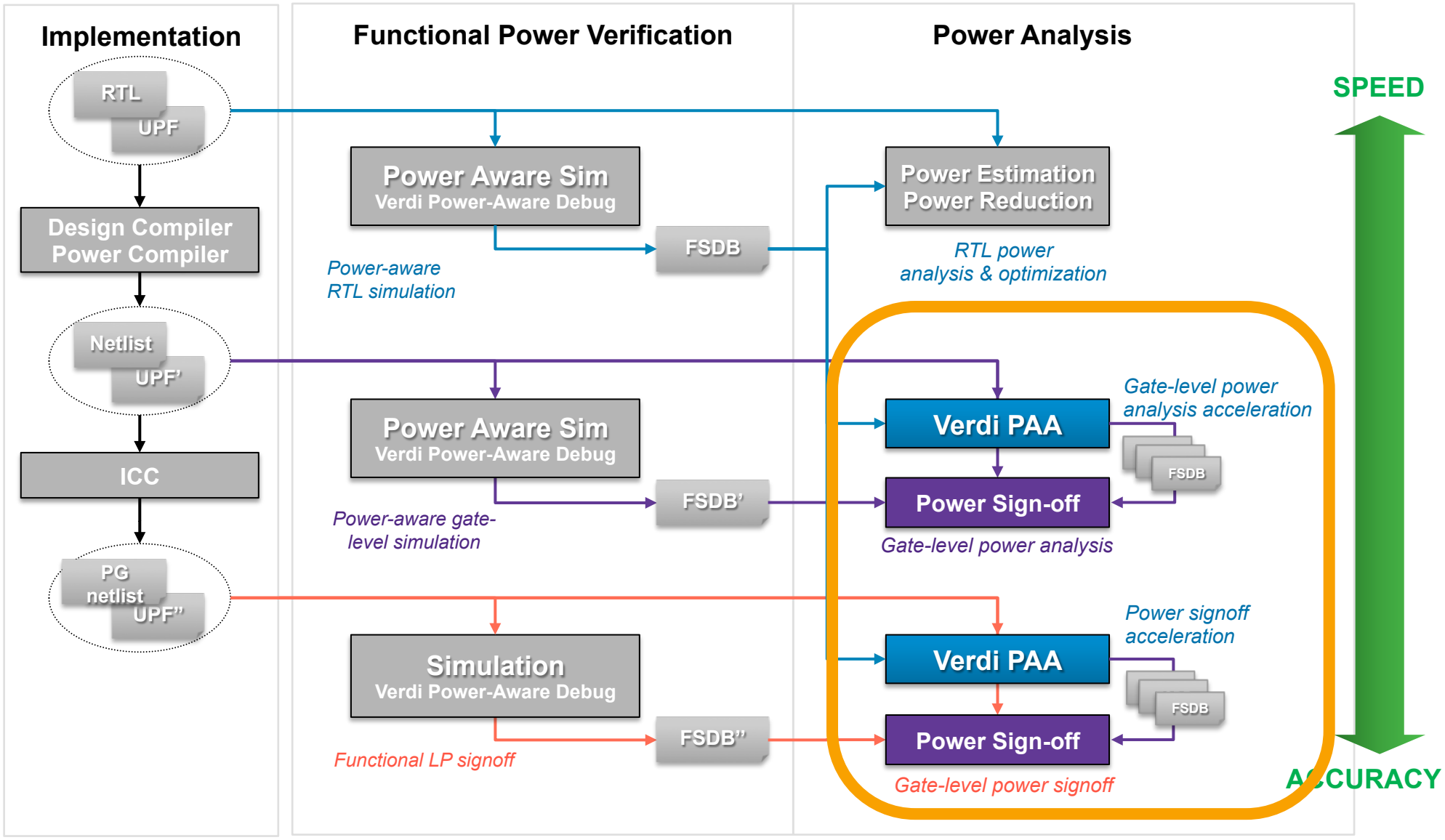
Power Clocks (3 power clocks) Full Expand

Clock	Frequency
mrx_clk_pad_i	12.562MHz
mtx_clk_pad_i	12.562MHz
wb_clk_i	33.333MHz

Note: Source of frequency obtained from simulation trace files (VCD,FSDB,SAIF,...etc)

Gate Level Power Analysis Acceleration

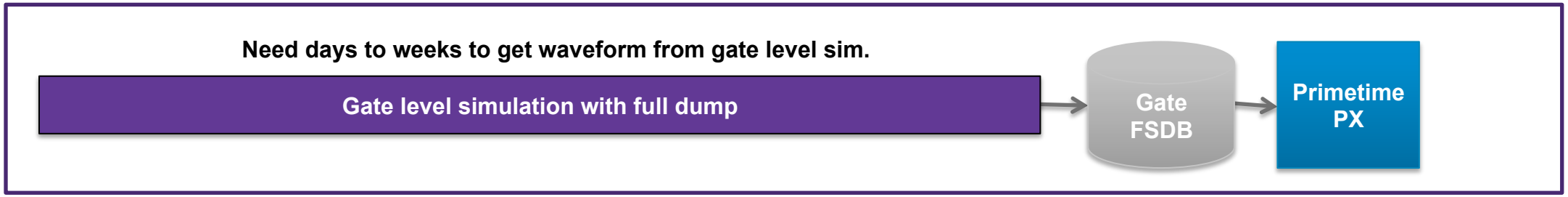
Synopsys Power Analysis Solutions



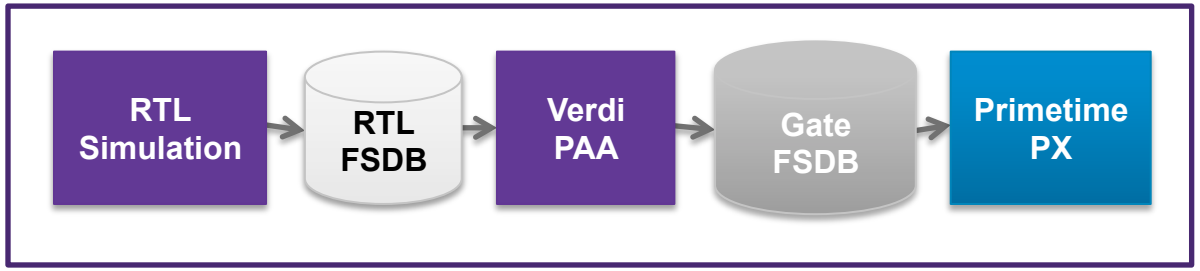
Power Analysis Acceleration Engine

Enable Gate Level Power Signoff with RTL Switching Data – Early and faster !!

Original Flow (Reference)



Verdi PAA Flow



Verdi Power Analysis Acceleration

- Estimate power before gate level env is ready
- Full range of gate level simulation is not required
- Leverage SDF to improve accuracy

	IDLE mode period		Active mode period	
	Reference	Verdi PAA	Reference	Verdi PAA
Simulation Run time	42 hrs	2 hrs	126 hrs	6 hrs
Time Saving		21X		21X
Total Power (mW)	0.0034	0.0033	0.0729	0.0713
Total Power Tolerance		0%		-2%

21X speedup
2% difference from reference flow

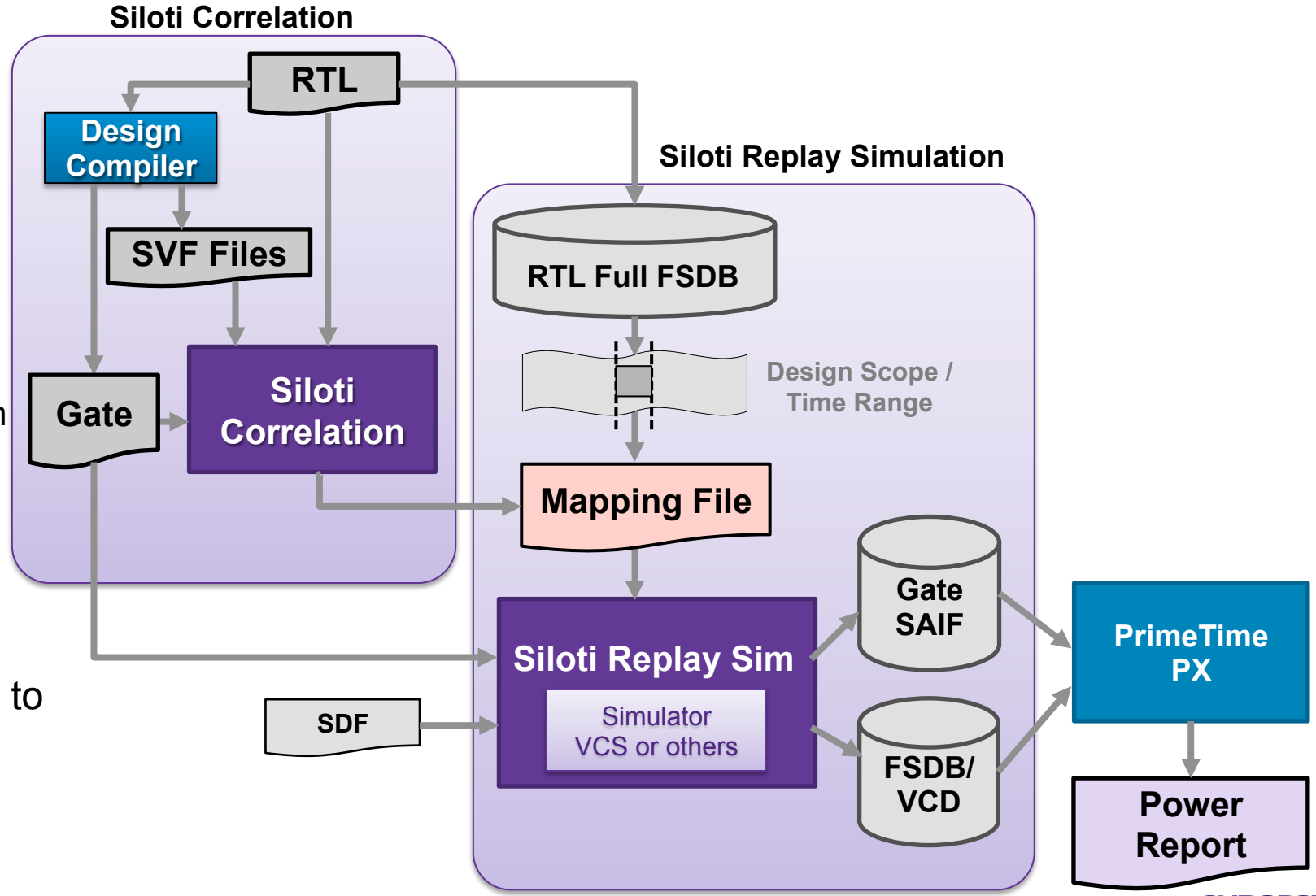
Power Analysis Acceleration

Uses Siloti Correlation and Siloti Replay Simulation with PrimeTime PX

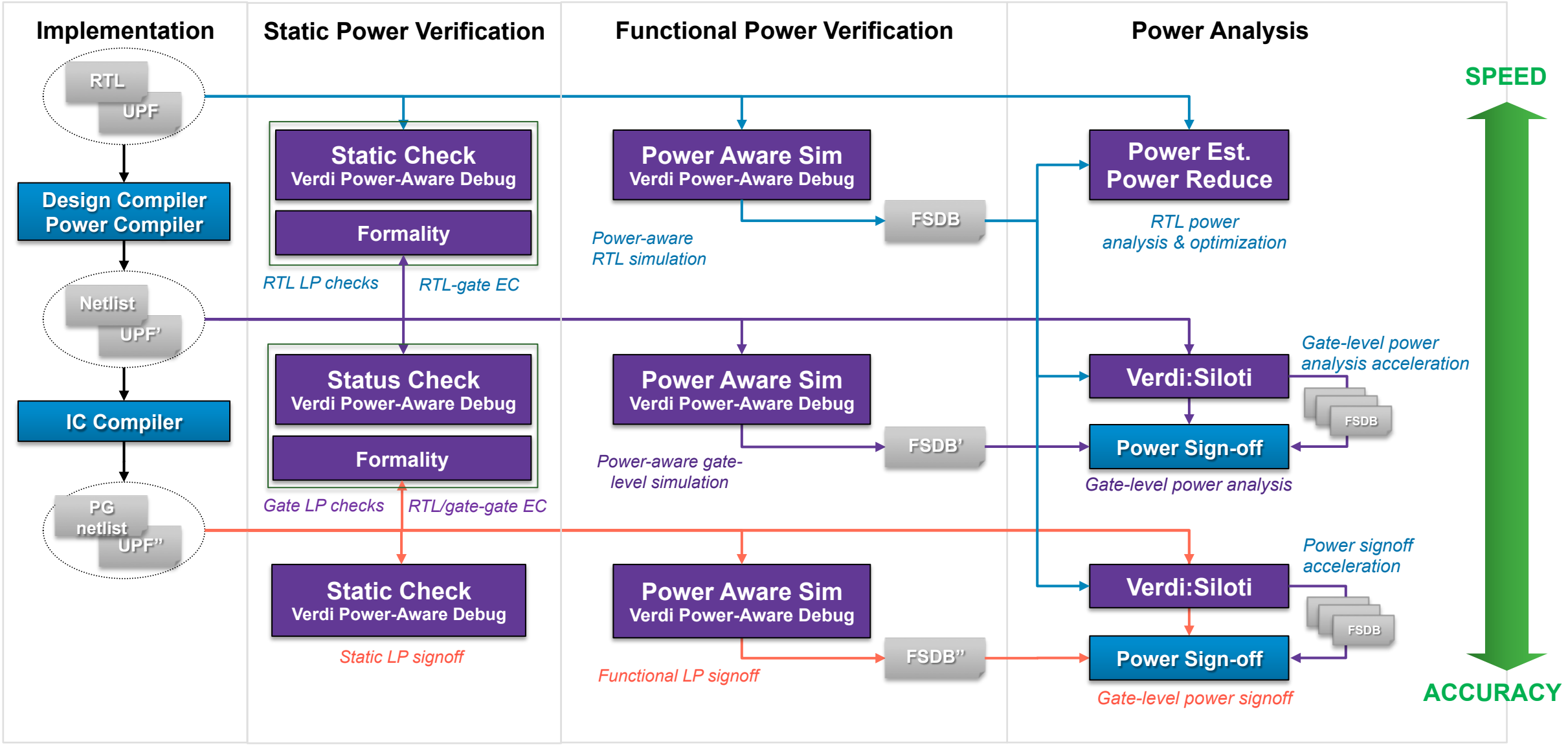
1. Siloti Correlation
   - Input RTL and netlist designs
   - Leverage SVF output from DC
   - Generate mapping file

2. Siloti Replay Simulation
   - Input FSDB from RTL simulation
   - Restrict simulation & dumping
   - Leverage SDF
   - Regenerate gate-level data

3. Input gate SAIF or FSDB/VCD to PrimeTime PX



Synopsys Power Verification & Analysis Solutions



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Q & A

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Thank You