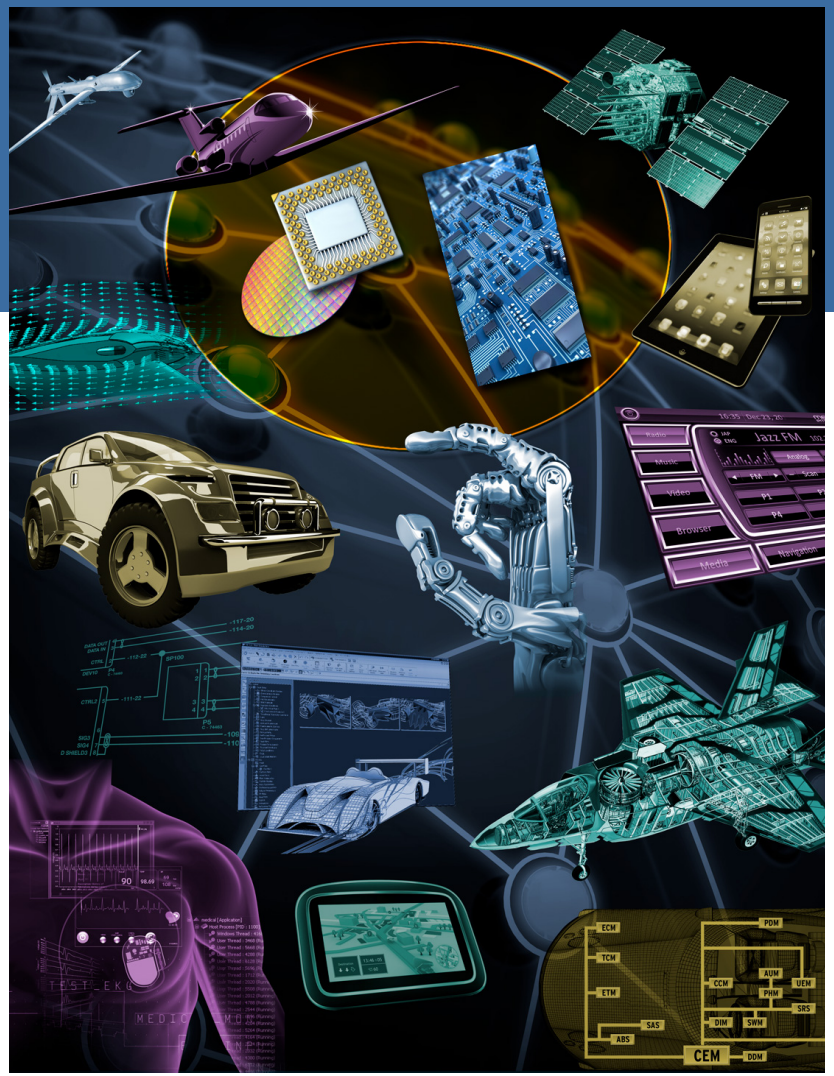
Verify Tomorrow's Systems: The Impact on Standards and Methodologies



Dennis Brophy

Director of Strategic Business Development

IC Verification Solutions Division

April 21, 2017

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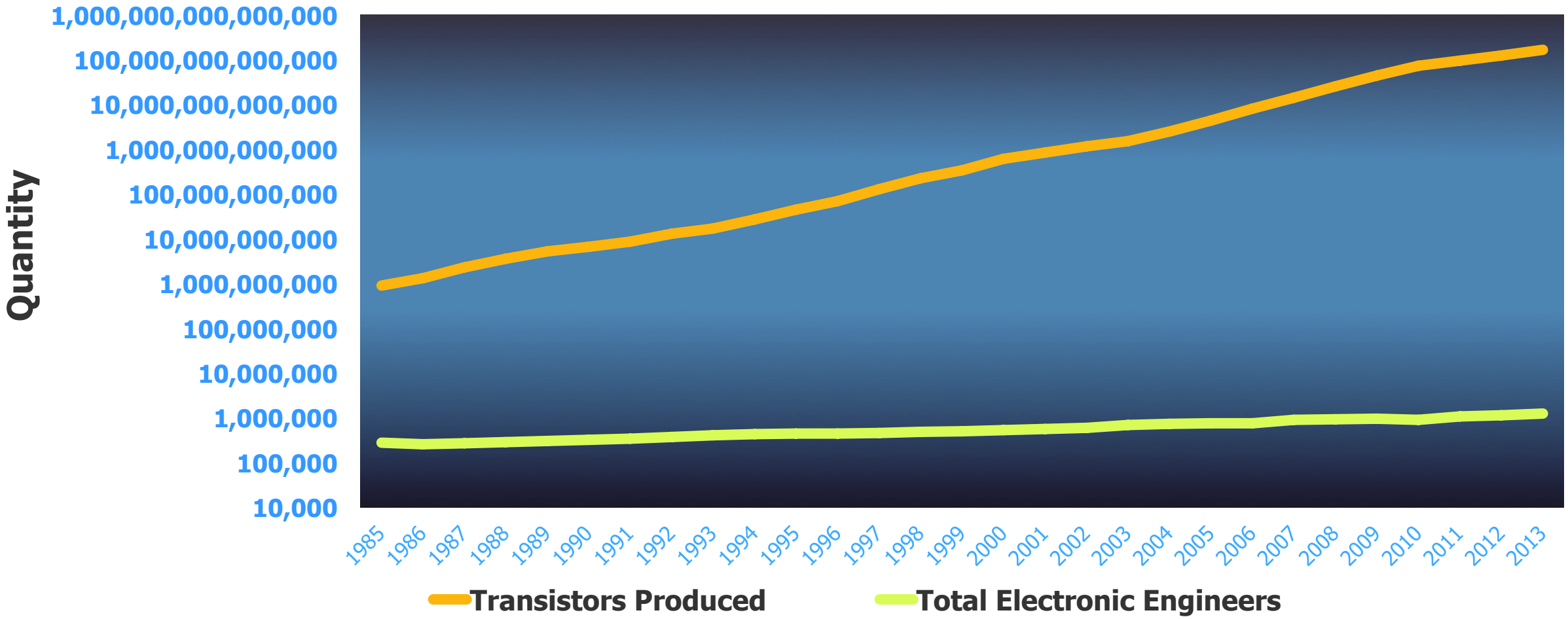
DESIGN PRODUCTIVITY

Design Productivity Grew 5 Orders of Magnitude Since 1985



Source: Technology Research Group – EDA Database, 1986, EDA TAM, 1989 & Gartner/Dataquest 2005 Seat Count Report, Gary Smith EDA, 2013 Seat Count Analysis, VLSI Research, 2013 - Transistors Produced Analysis

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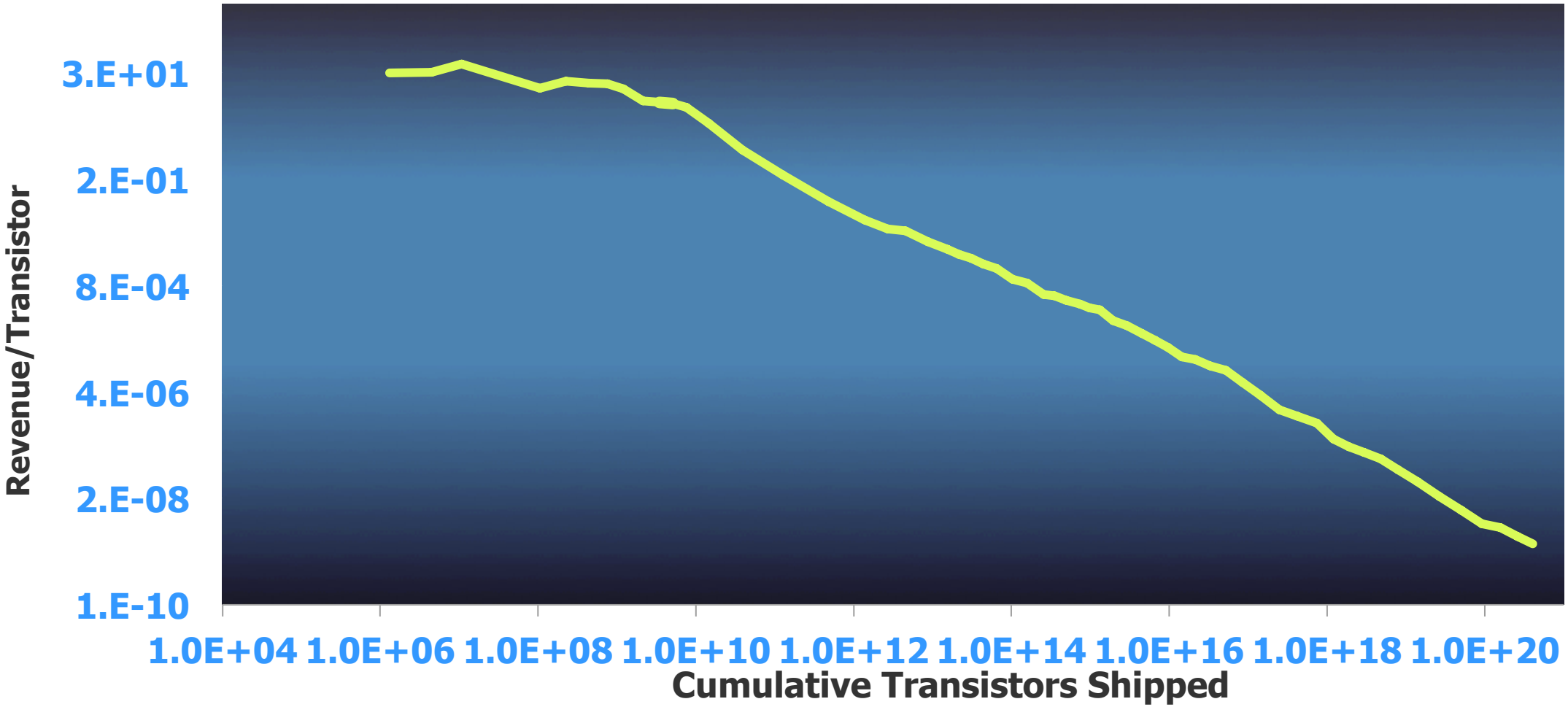
Cost Learning Curve Continues With or Without Moore's Law



Semiconductor Learning Curve 1954-2012 Adjusted for Inflation

Source: VLSI Research, SIA, Federal Reserve *Note: Revenue adjusted for Inflation… 1954-2012*

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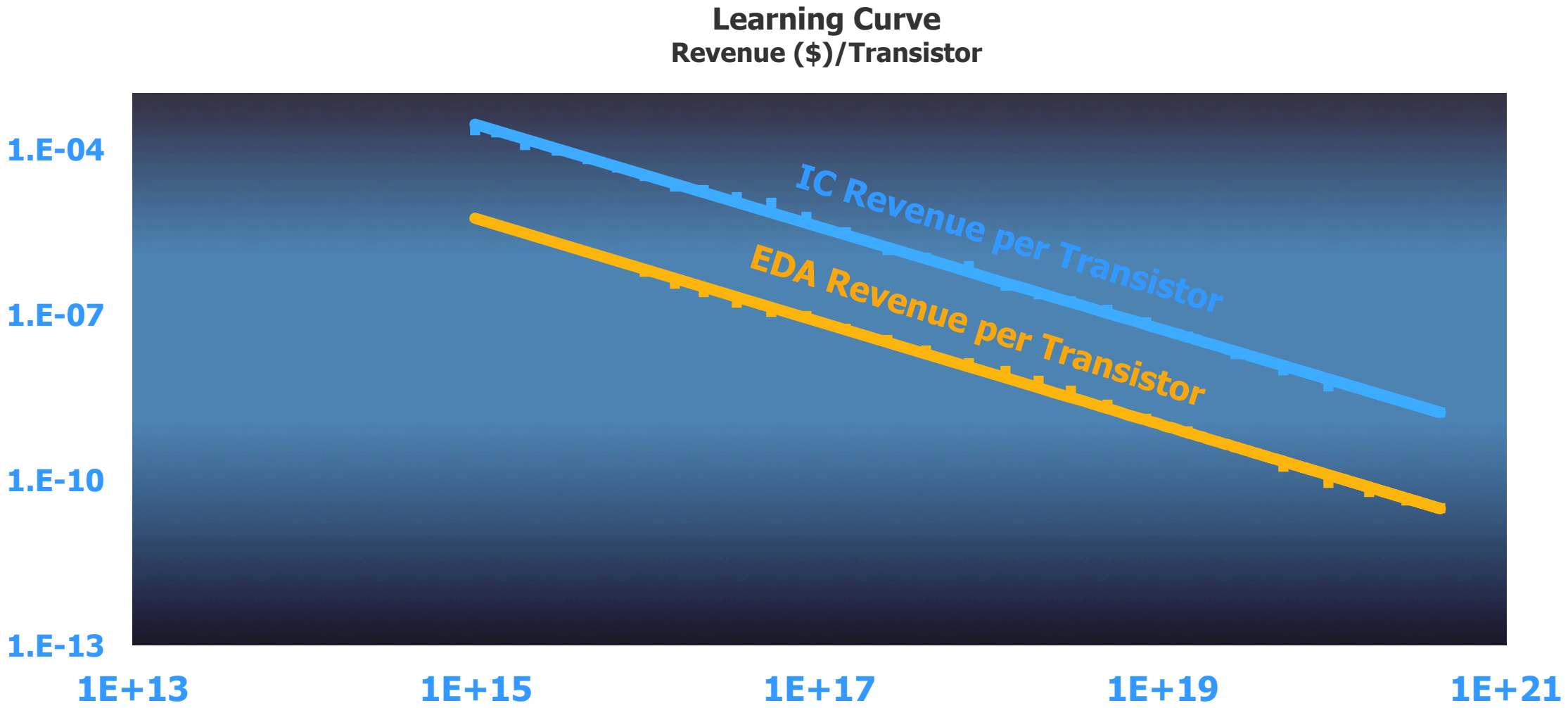
Cost of EDA Software Decreases at the Same Rate as the Revenue per Transistor



Note: EDA Cost Consists of EDA License and Maintenance revenue adjusted for Inflation

Source: VLSI Research, EDAC Market Statistics Service, Federal Reserve

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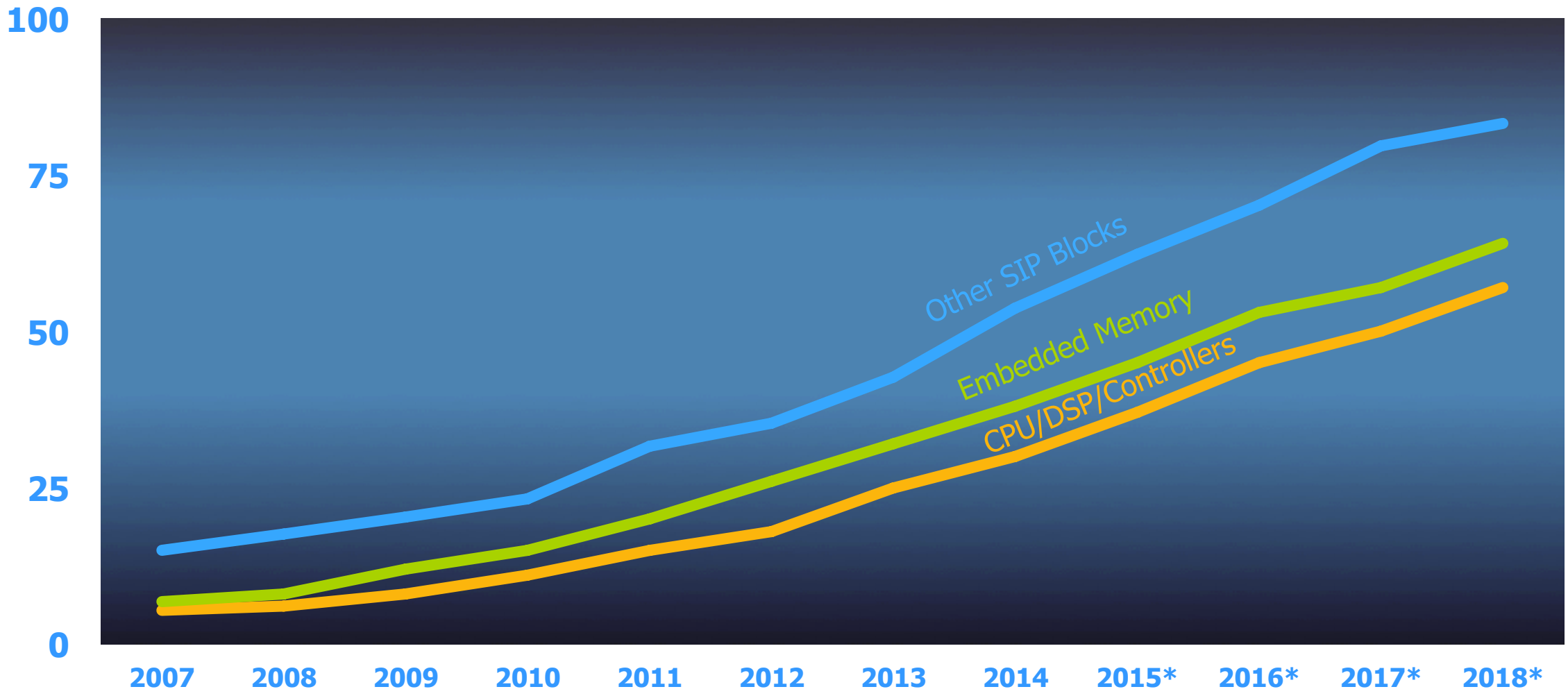
IP Reuse Has Driven a Large Share of Recent Design Productivity Gains



*Source: Semico Research Corp. *Forecast*

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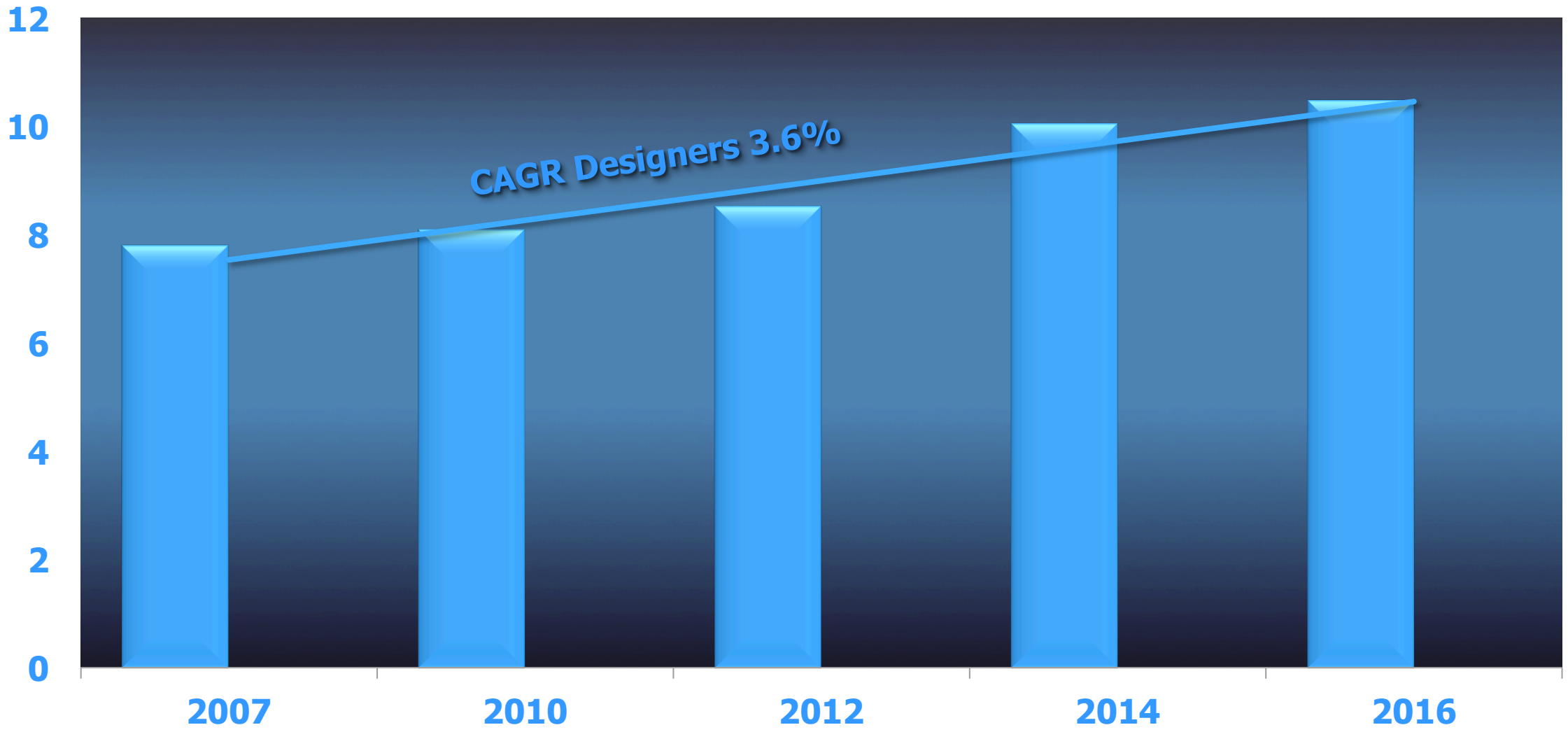
Demand for Design Engineers Grows Slowly



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

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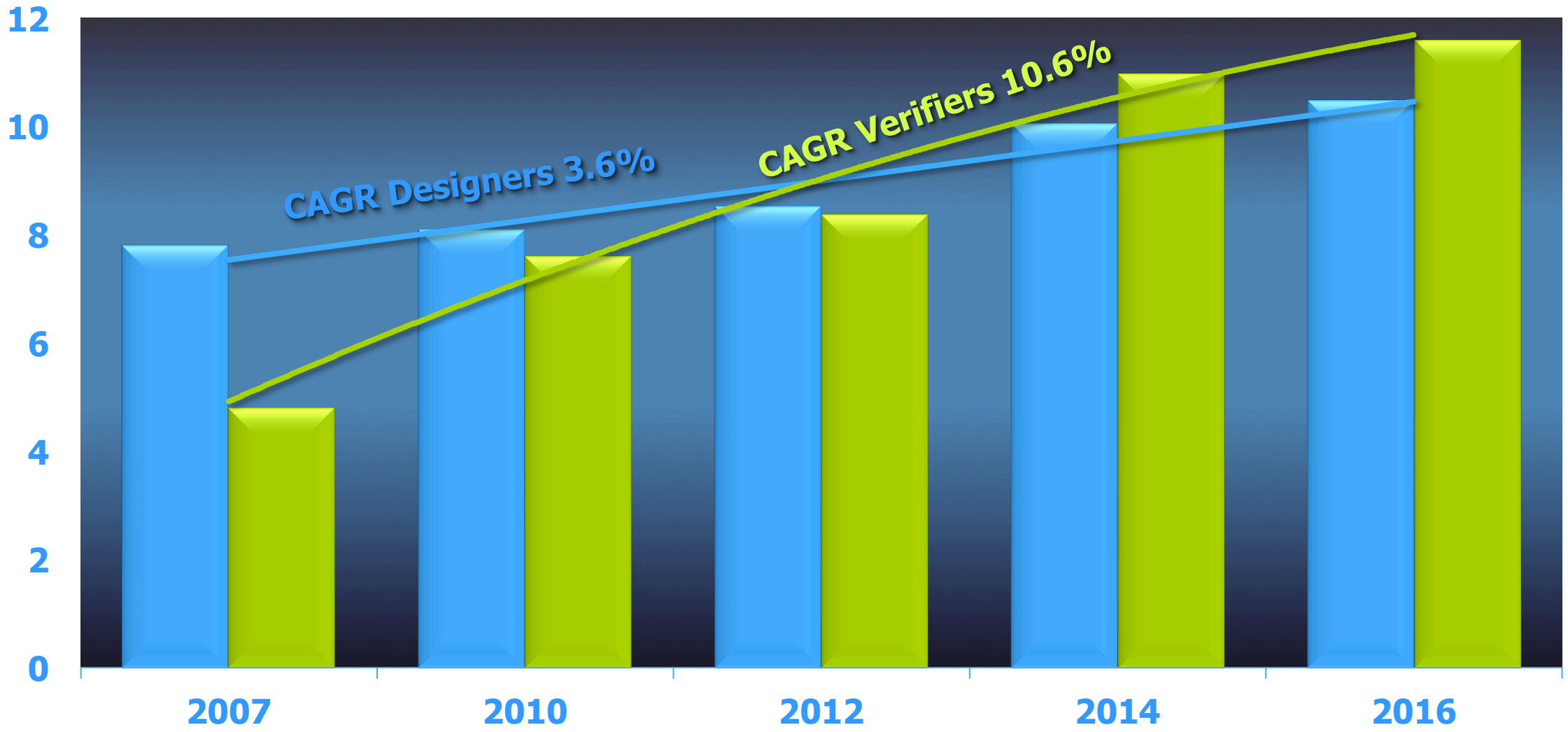
Verification Engineers Increase at 3X the Rate of Increase of Designers



Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study

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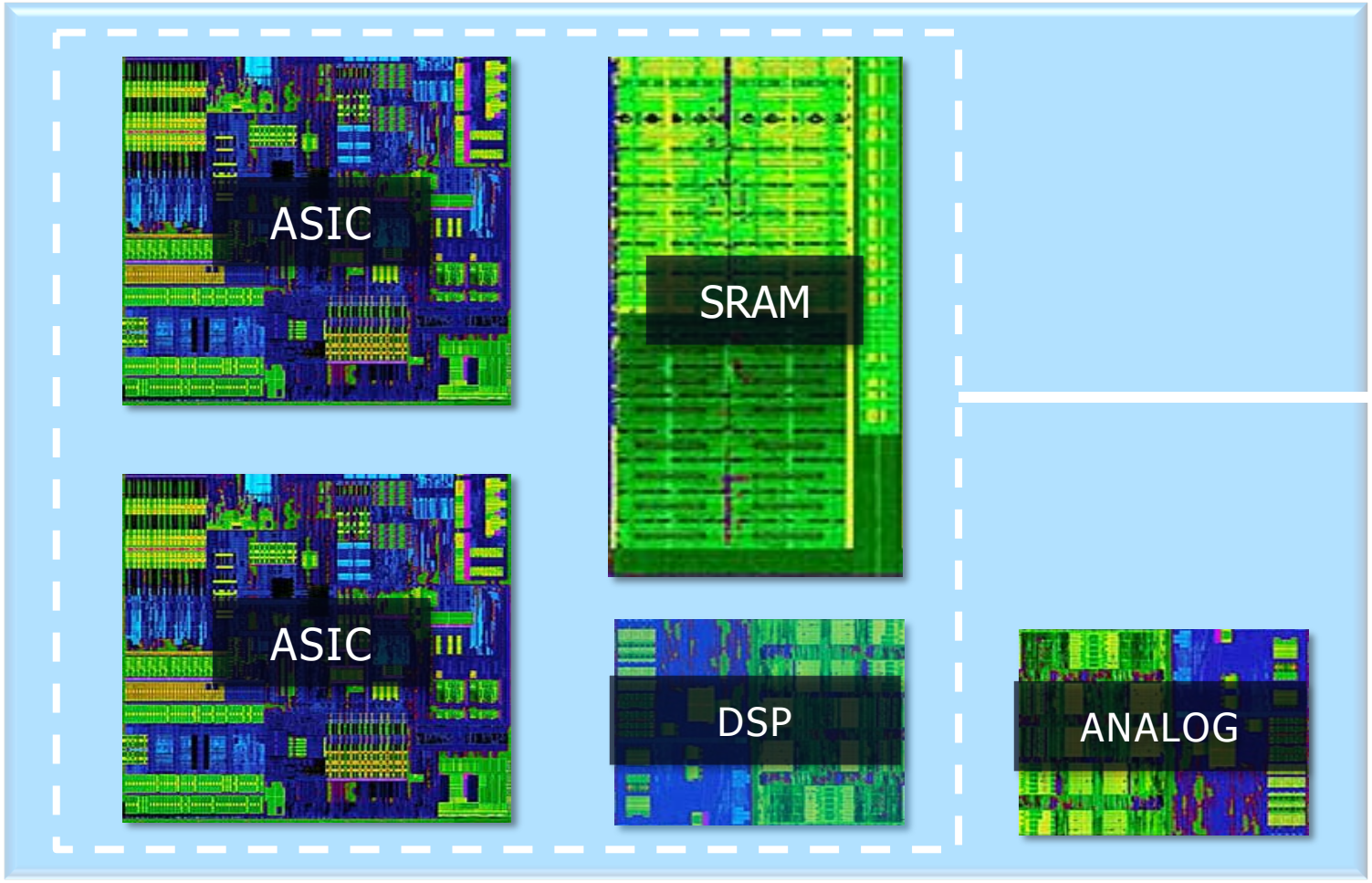
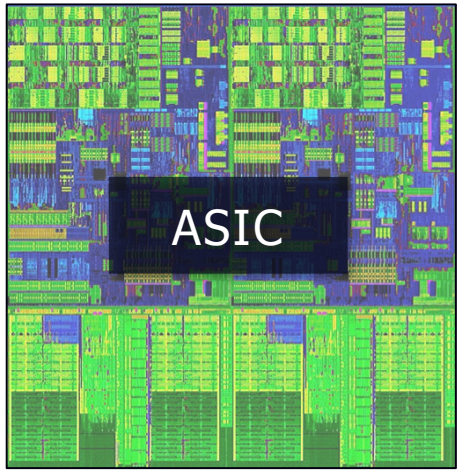
Upper Bound of Verification Cycle Requirements Increases 2^x





x = memory bits + flip-flops + latches + I/O

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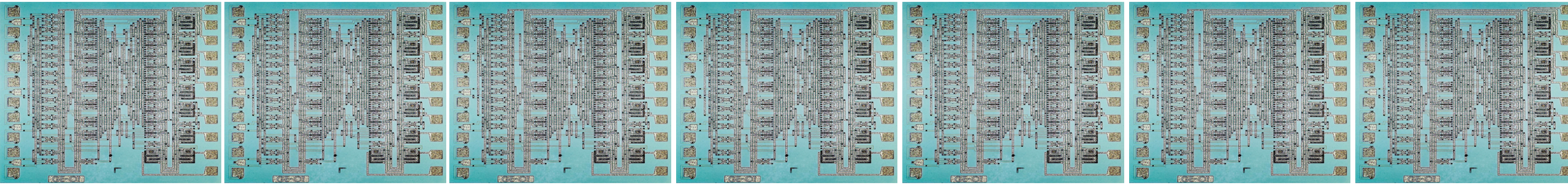
HOW DID WE GET HERE?
A LOOK BACK...

Large Scale Integration (LSI) Evolves to VLSI

- SSI/MSI design and verify
  - Manual design and layout
  - Fabricate it
  - Test it
  - Re-design it
  - Repeat



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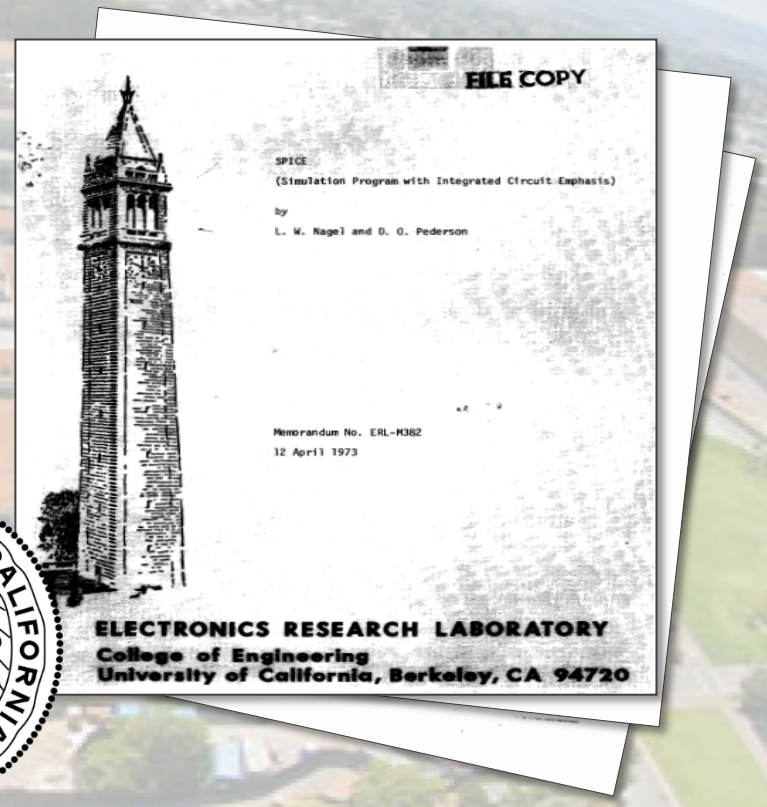
Transistor-Level Simulation

- **CANCER**
  - Ron Roher
- **SPICE** – Simulation Program with Integrated Circuit Emphasis
  - L.W. Nagel and D.O. Pederson
  - Presented April 12, 1973



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Larger Designs Required Gate-Level Simulation

Mentor Graphics – 1982
IDEA Station – QuickSim

QuickSim

Performance:

Workstation dependent

Capacity:

Workstation dependent

100K+ gates when gate-level models are used, much larger when functional or behavioral modeling methods are used

Source: Mentor Graphics

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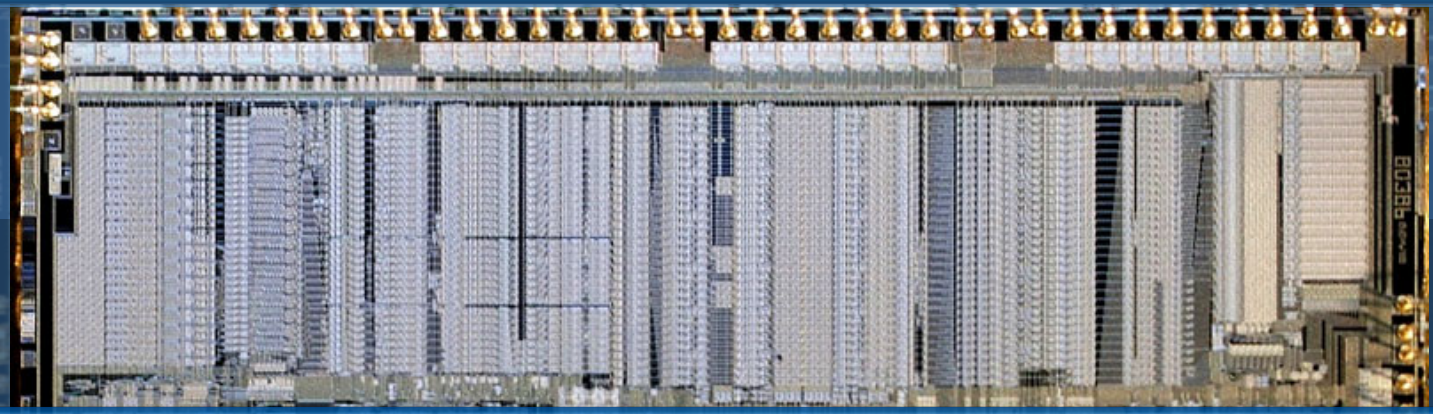
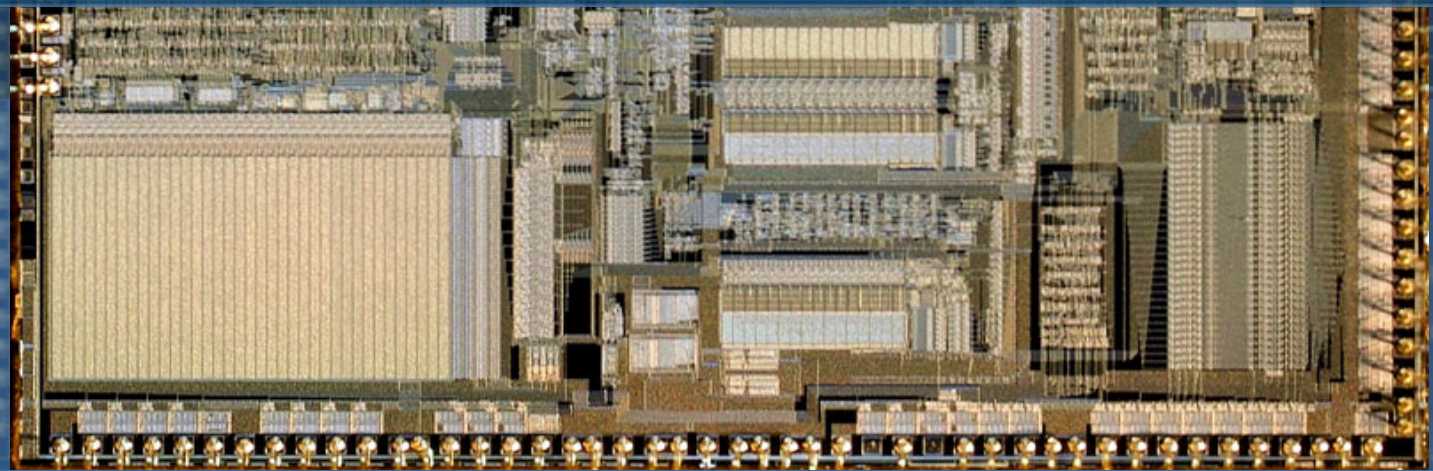
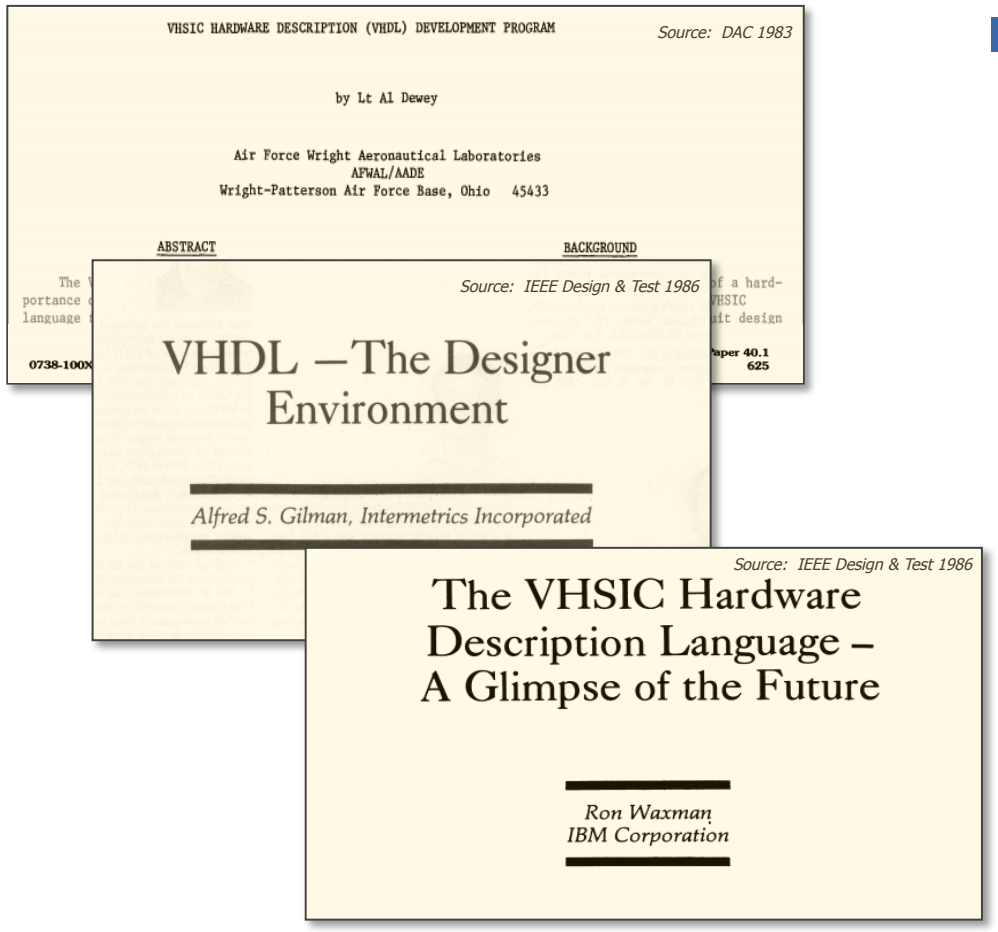


RTL ERA

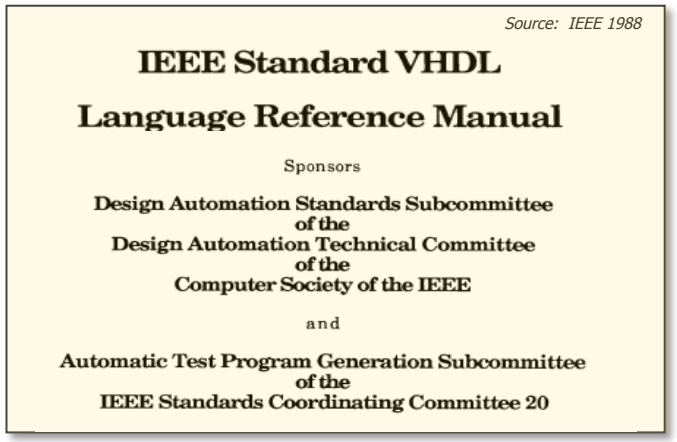
Focus on Languages and Improving Performance



VHDL Hardware Description Language



- IBM, Texas Instruments & Intermetrics awarded contract – 1983
  - VHSIC Hardware Description Language
  - VHDL 7.2 released in 1985
  - VHDL became IEEE Standard 1076 in 1987



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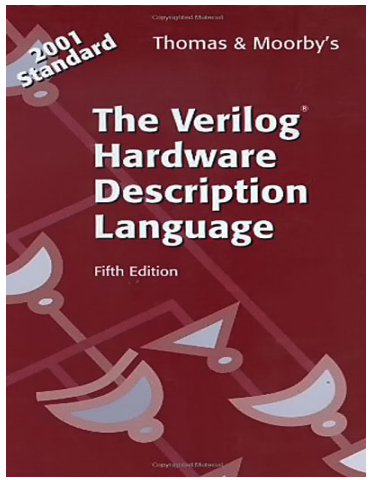
Verilog Hardware Description Language

- Gateway Design Automation – 1985
  - Verilog HDL created by Phil Moorby in 1984
  - Acquired by Cadence in 1989
  - Verilog became IEEE Standard 1364 in 1995



Source: IEEE Design & Test of Computers, August 1985

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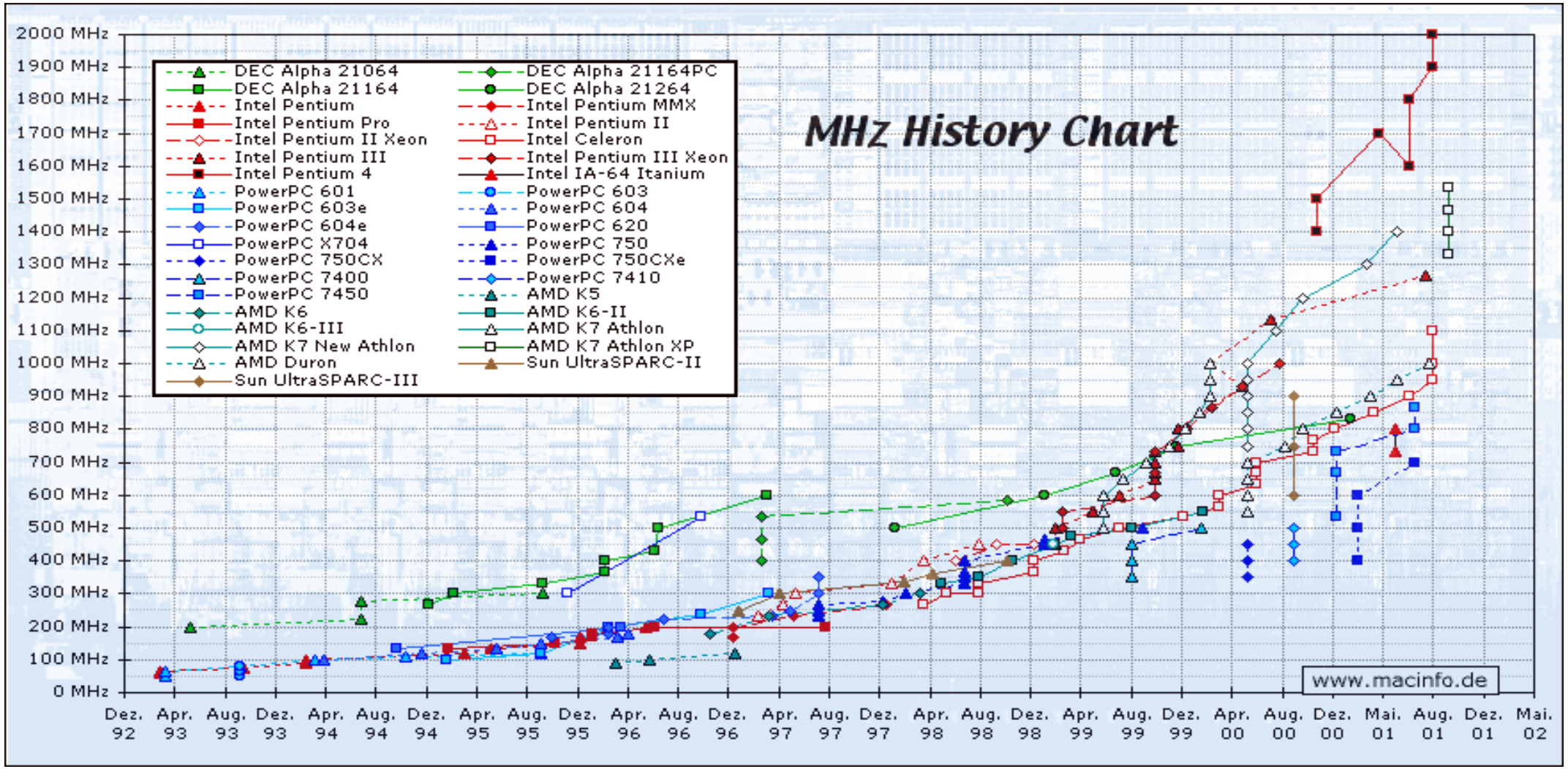
Ever-Improving Compute Performance



Source: www.macinfo.de

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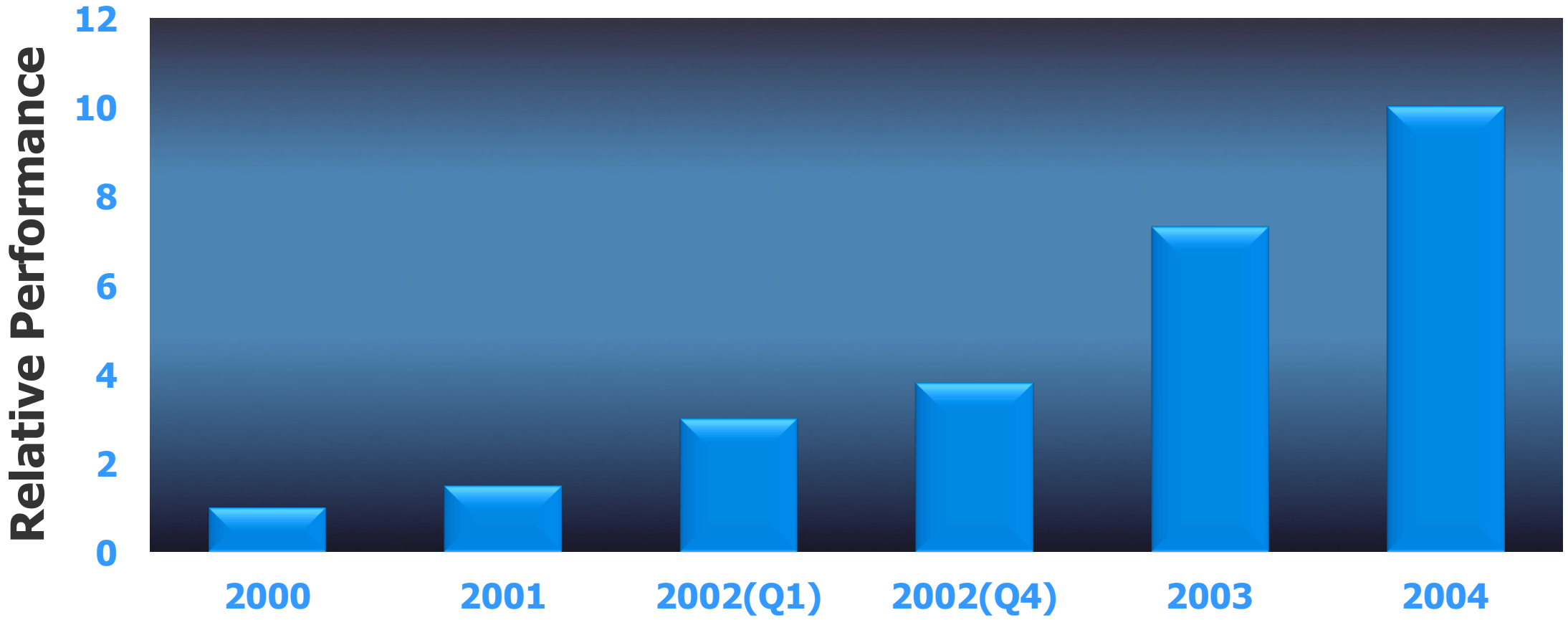
RTL Simulation Accelerates Independent of Hardware Performance



Source: Mentor Graphics

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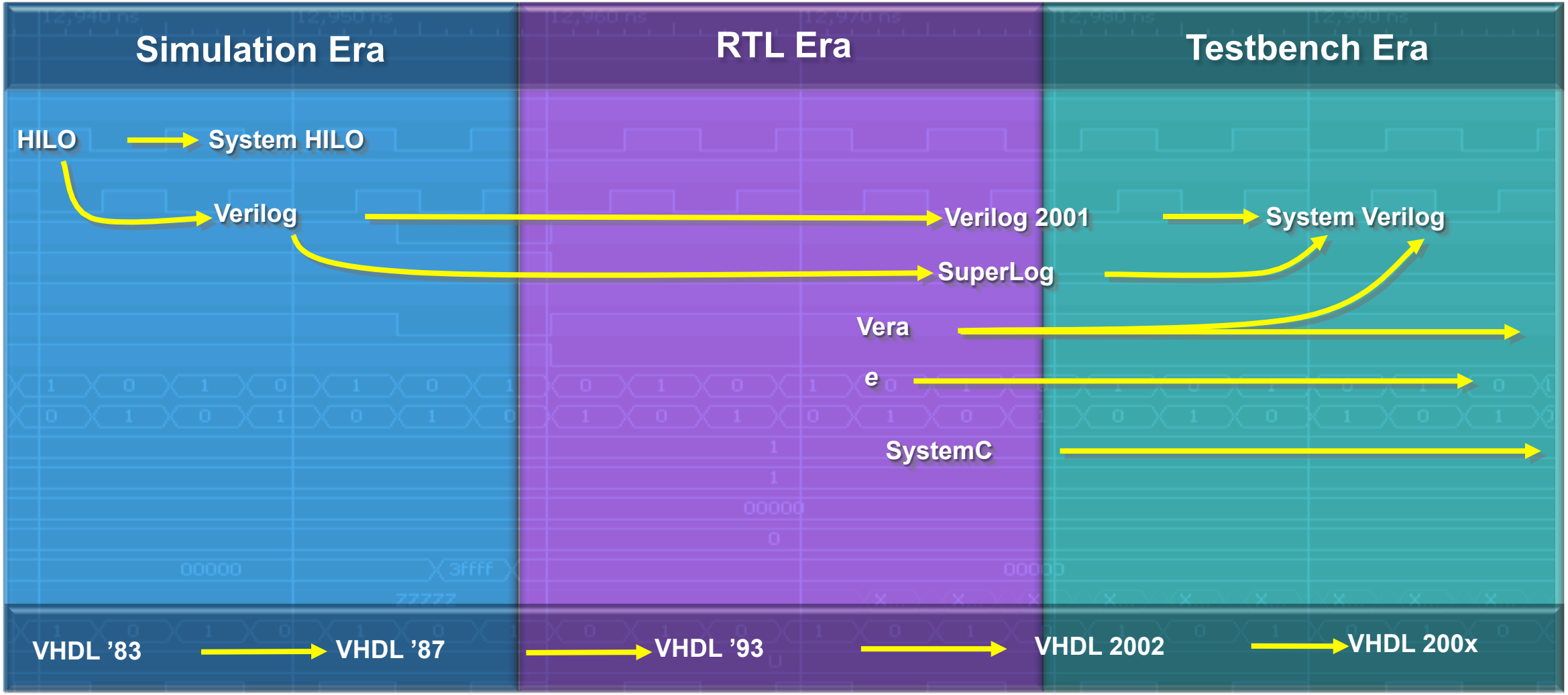
Verification 2.0

TESTBENCH AUTOMATION FOCUS ON METHODOLOGIES

Language Evolution



Source: Mentor Graphics

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Industry Converges on IEEE 1800

EE Times

IEEE unifies Verilog standards efforts

Richard Goering

6/24/2004 3:00 PM EDT

SANTA CRUZ, Calif. — Putting to rest fears of a Verilog language schism, the IEEE has decided to form a single working group that will encompass both SystemVerilog and the further evolution of the IEEE 1364 Verilog language standard.

The move follows criticisms of Accellera's decision to take SystemVerilog to a new IEEE working group rather than the existing 1364 committee.

In May, Accellera voted to take SystemVerilog to a new working group under the

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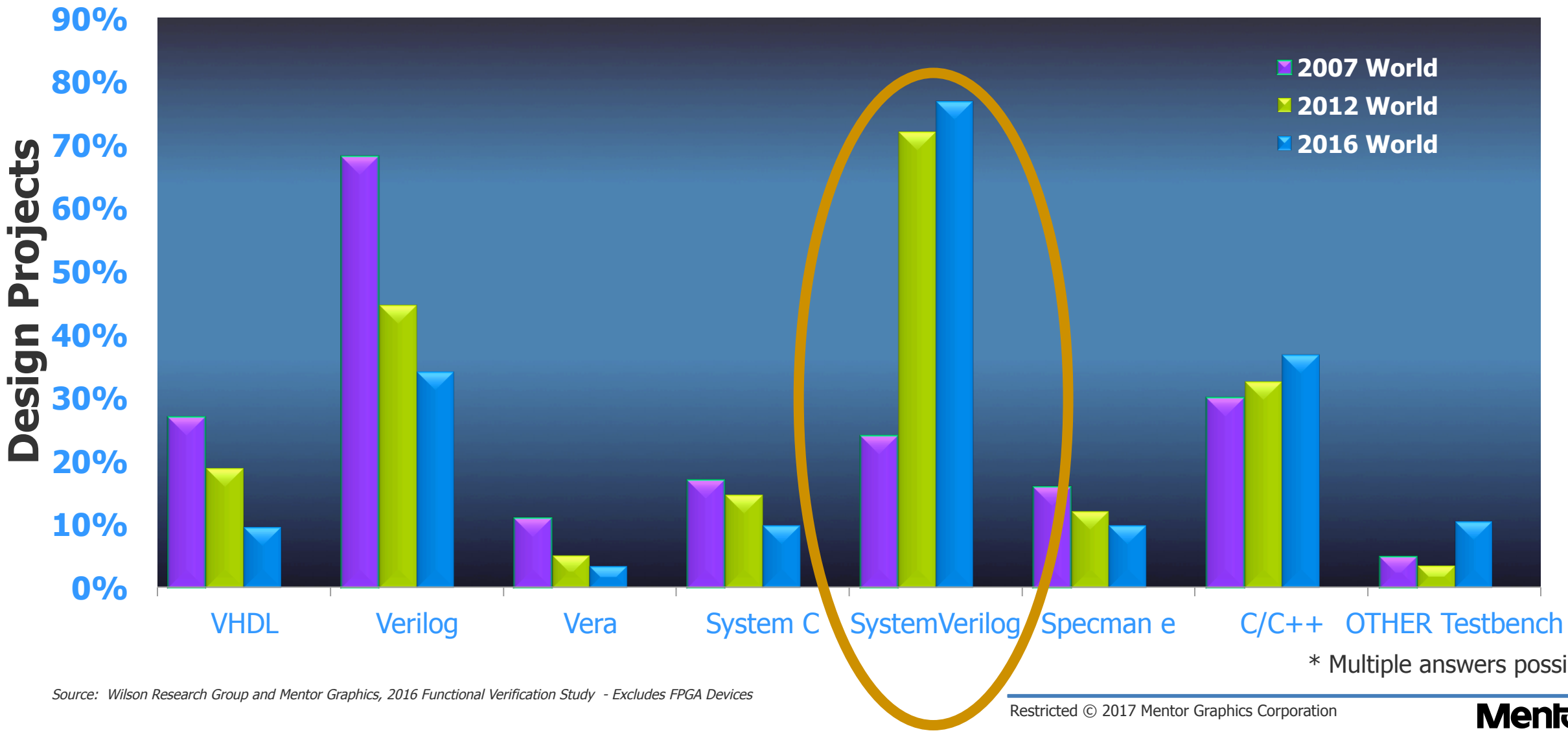
SystemVerilog Becomes Mainstream Verification Language



* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

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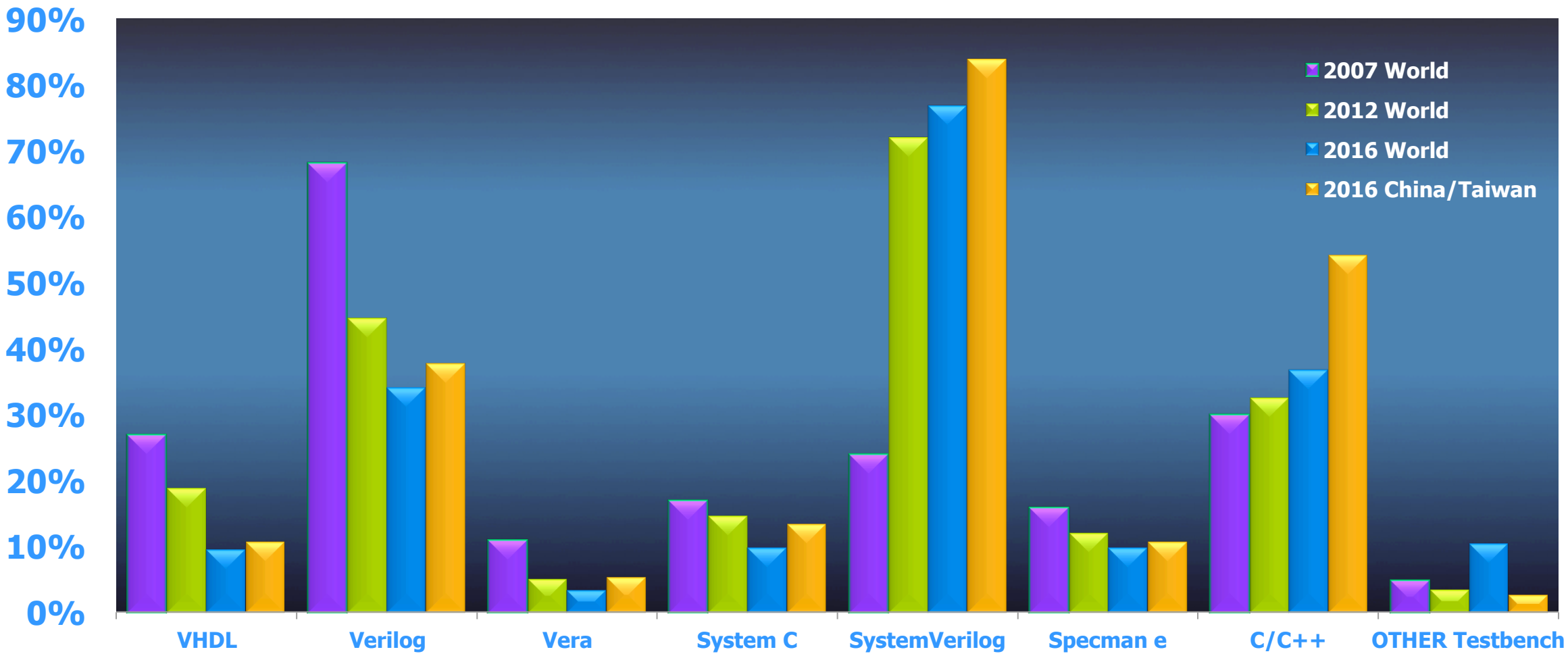
China/Taiwan a Leader in SystemVerilog Adoption



* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

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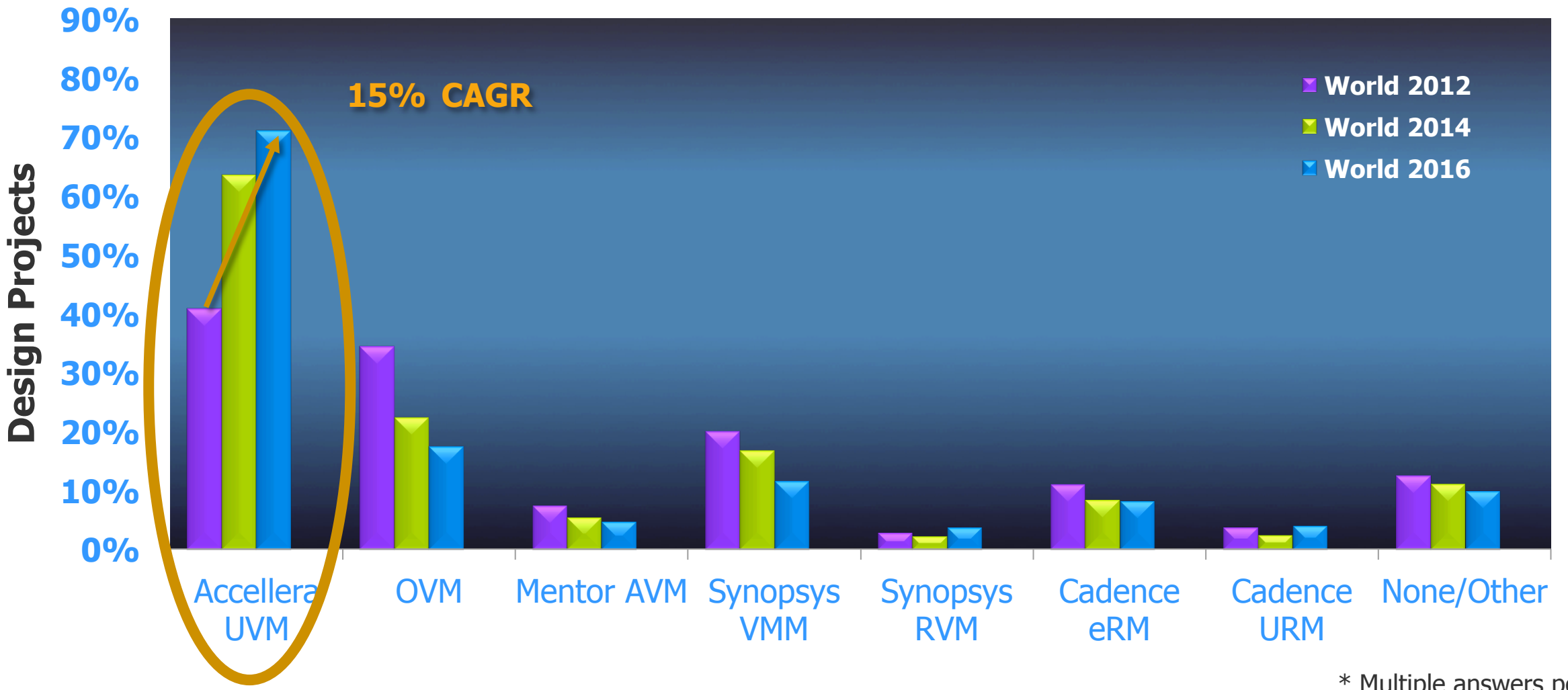
Class Library Standardization Around UVM



* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

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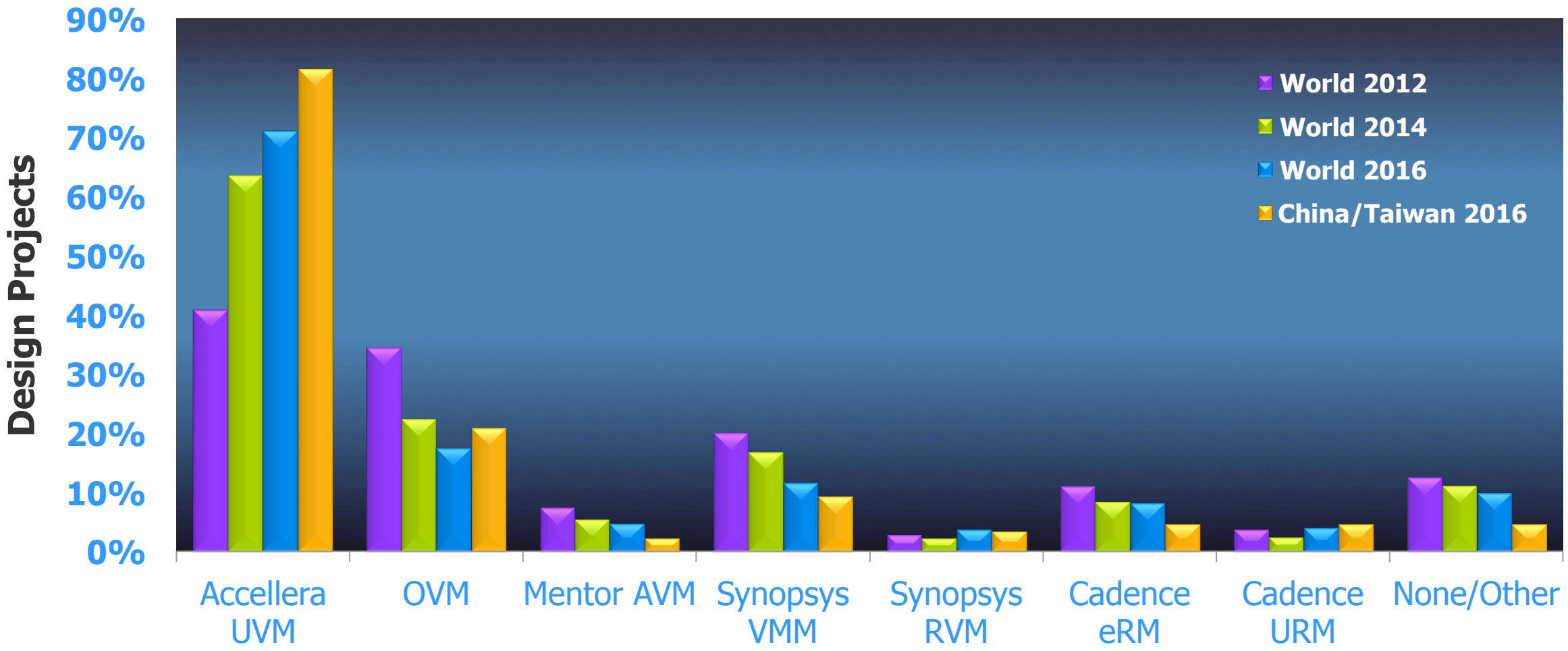
China/Taiwan a Leader in UVM Adoption



* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2016 Functional Verification Study - Excludes FPGA Devices

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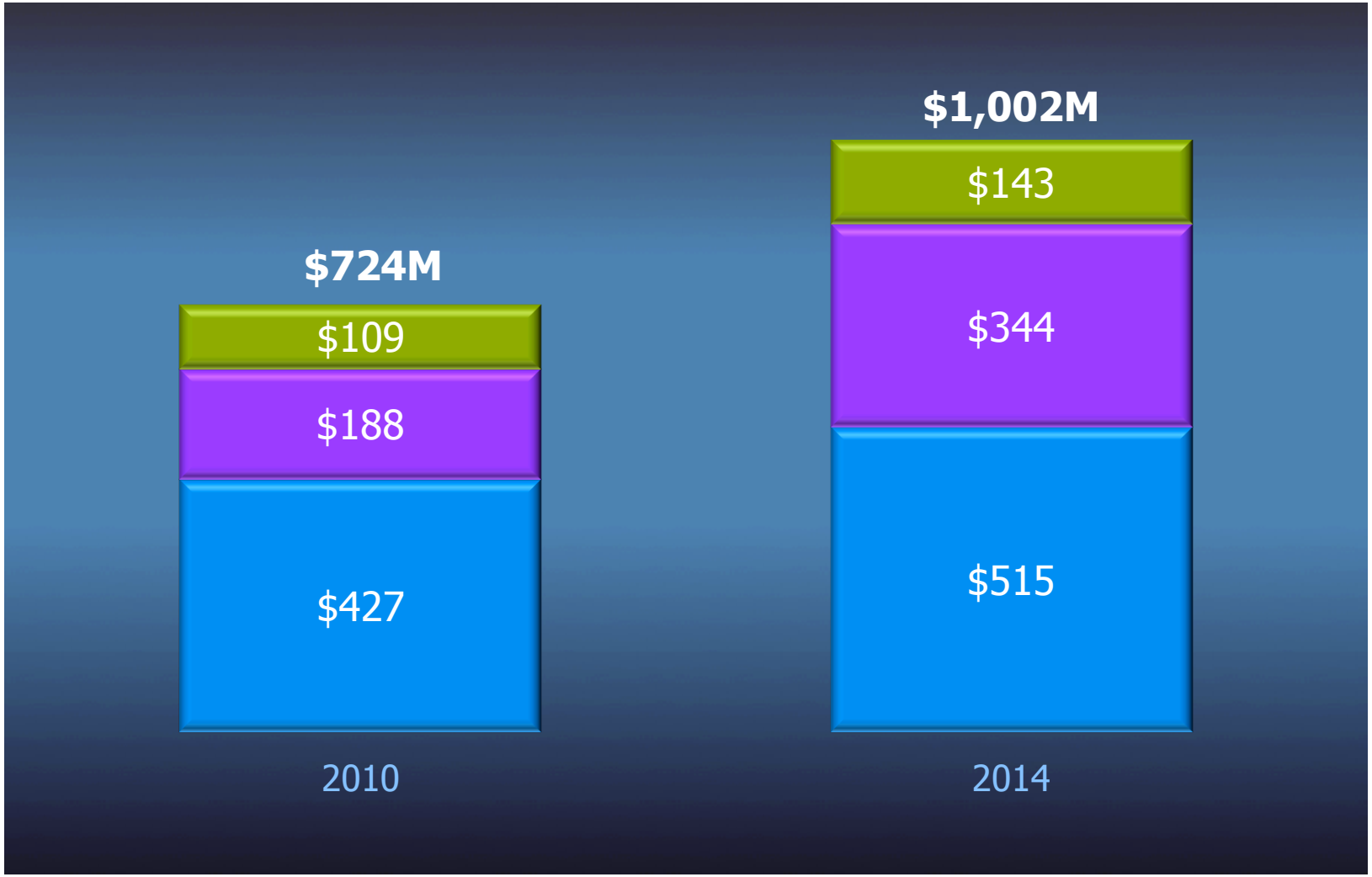
Verification Is a $1 Billion Market



2010-2014 CAGR
Total 9%

Formal 7%

Emulation 16%

Simulation* 5%

**Includes dynamic RTL simulation tools*
Source: EDAC Market Statistics Service

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SYSTEM ERA

Integrating Cross-Domain Systems: An Automotive Example

Software

Market Drivers

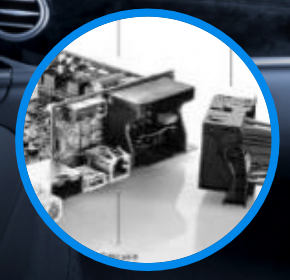
Hardware Complexity

High Cost of Failure

IVI

Driver Information

ADAS

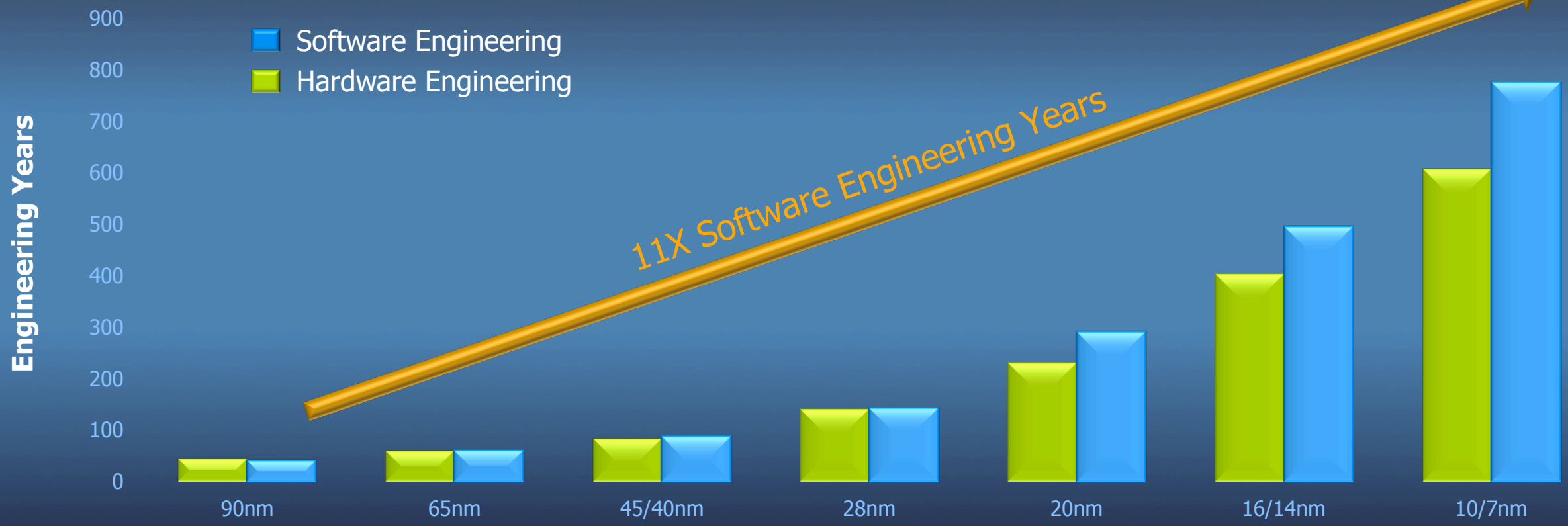


Telematics

Car Network

- Integrating cross-domain systems exposes emergent behavior earlier in the design process; Functional, Performance, Safety/Security, Connectivity

Embedded Software Development Headcount Surges past Hardware Design and Verification Headcount



Source: International Business Strategies, Inc. (IBS), 2015

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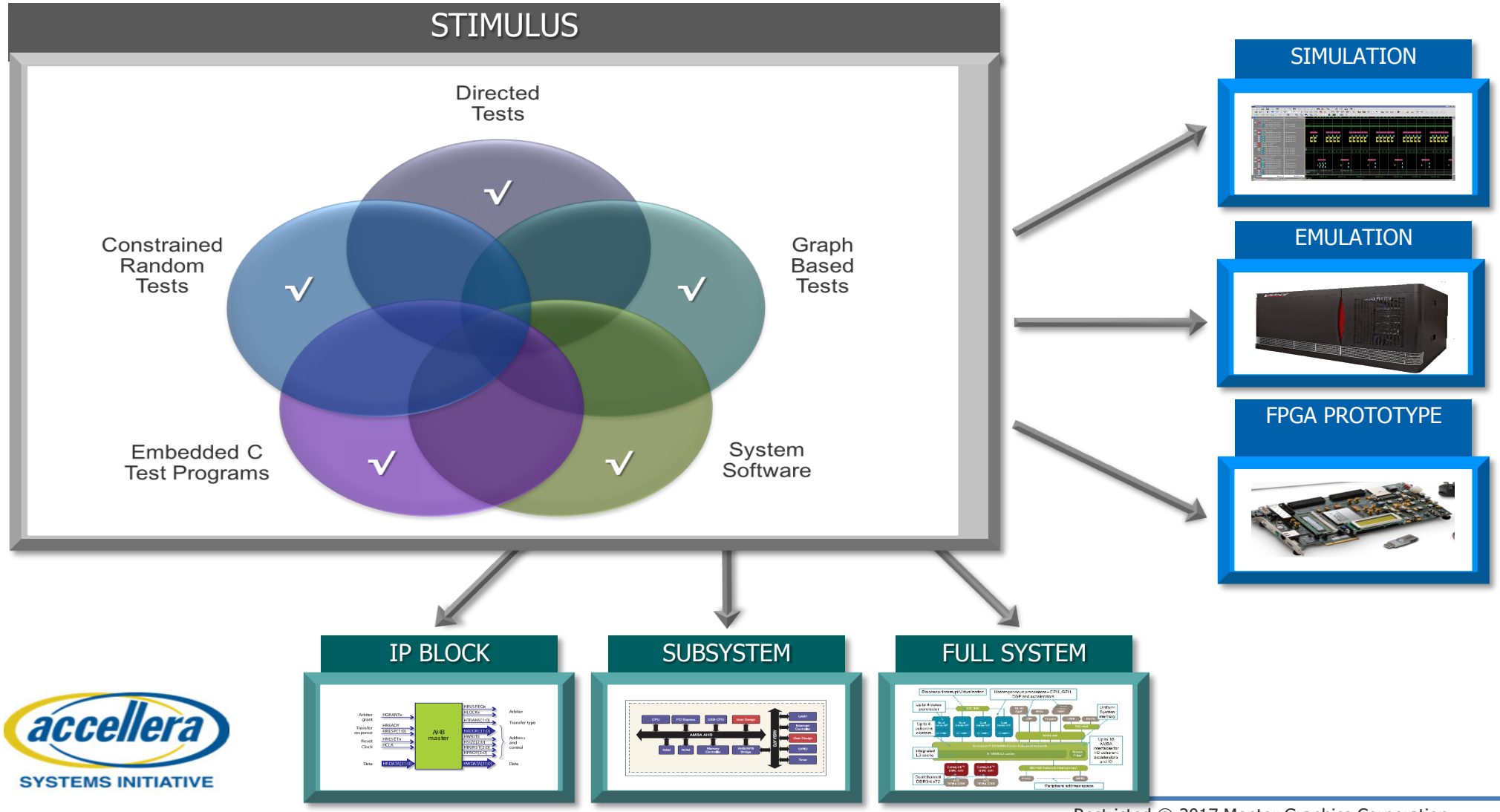
WHAT'S NEXT FOR SYSTEM ERA?

Improved Stimulus Generation with Portable Stimulus



accellera SYSTEMS INITIATIVE

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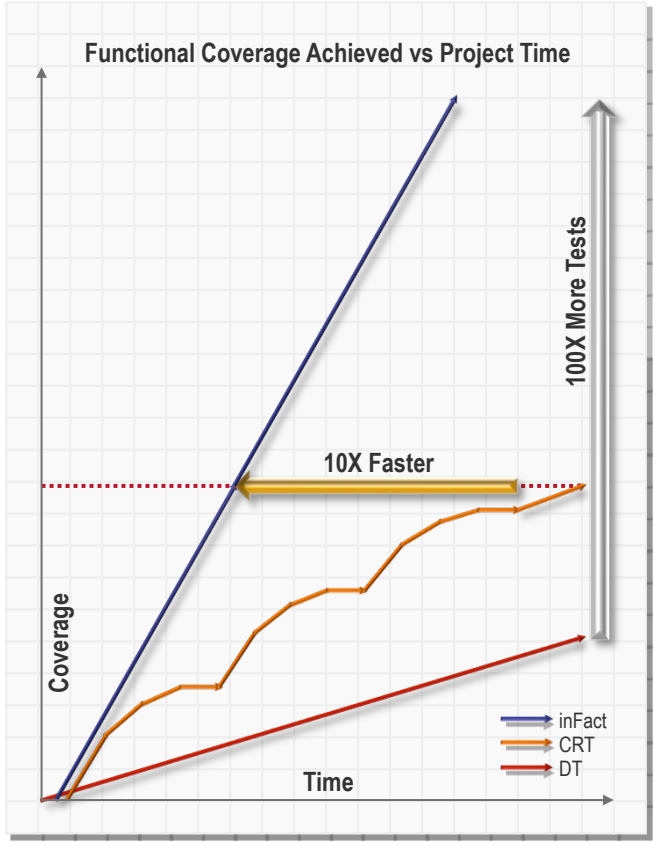
Supporting Portable Stimulus Technology

- Accelerates Coverage Closure
  - No wasted stimulus
  - 10-100x faster ramp to coverage goals
  - Fewer simulation resources
- Expands Directed Tests
  - Re-use existing stimulus description
  - Generate even more tests
  - Boosts verification comprehensiveness
- Integrates Easily
  - Flexible testbench environment support
  - Non-invasive integration
  - Reuse existing BFMs/checkers



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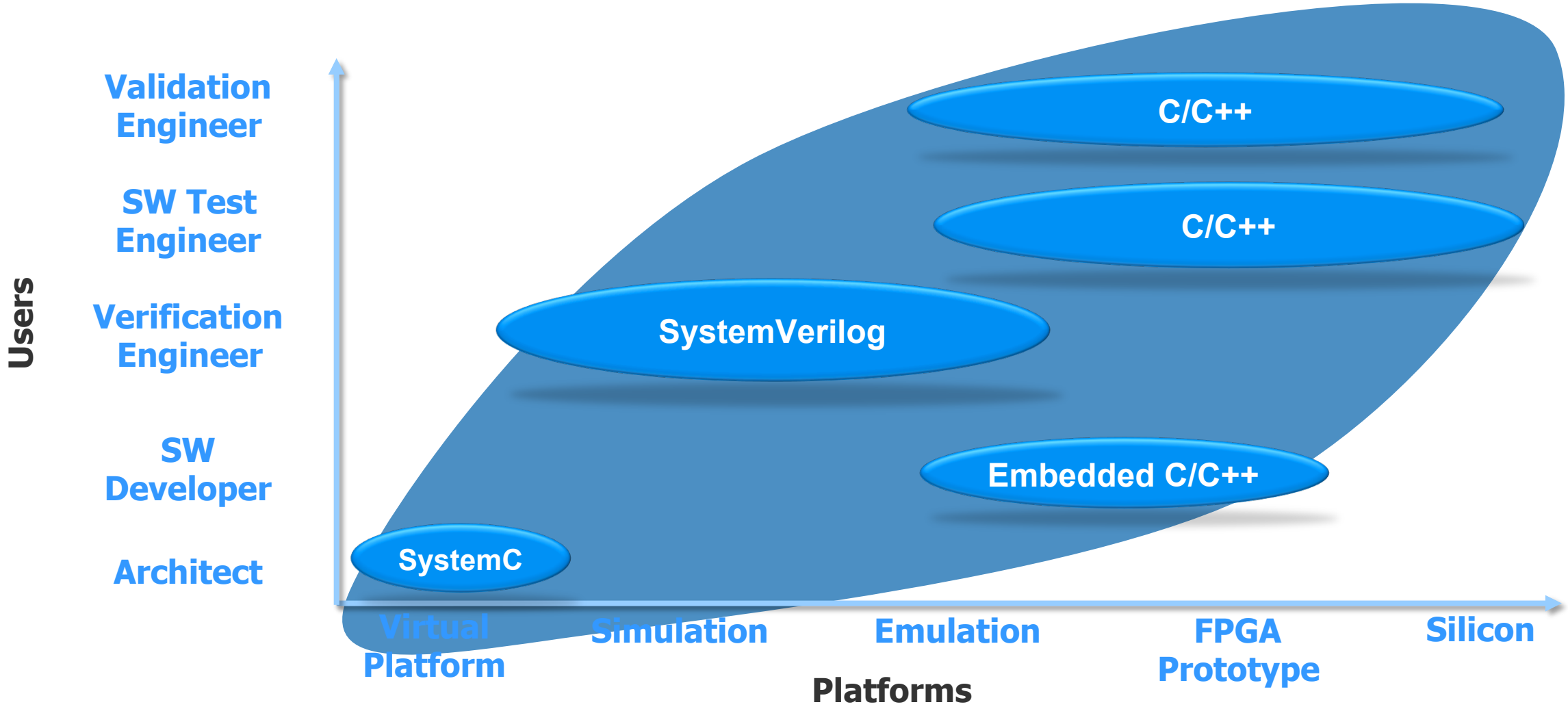
Evolution of the Portable Test Bench



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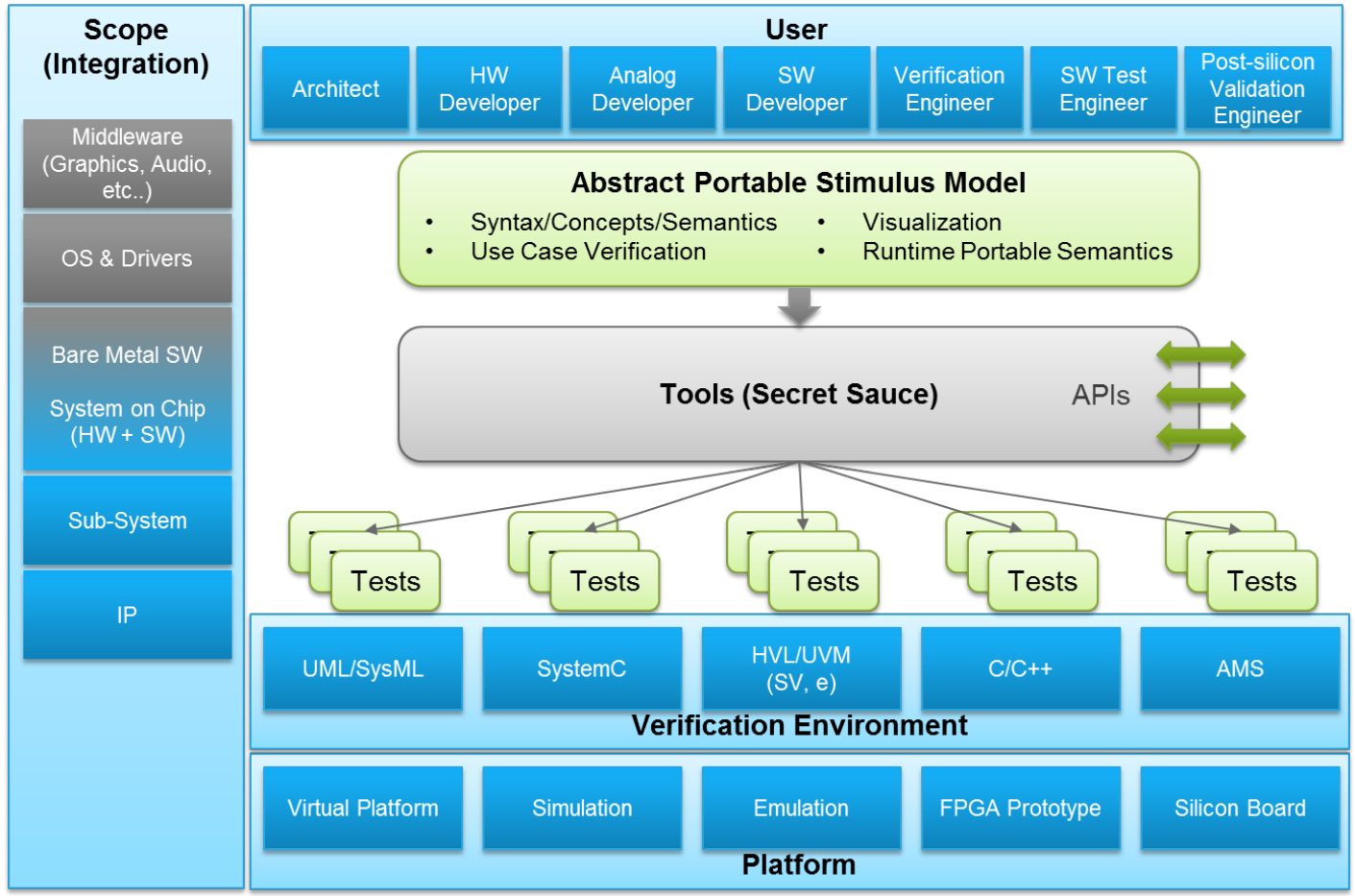
Portable Stimulus Working Group

- Single input specification
- Enable test creation automation
- Reusable across all platforms
- Tools generate specifics



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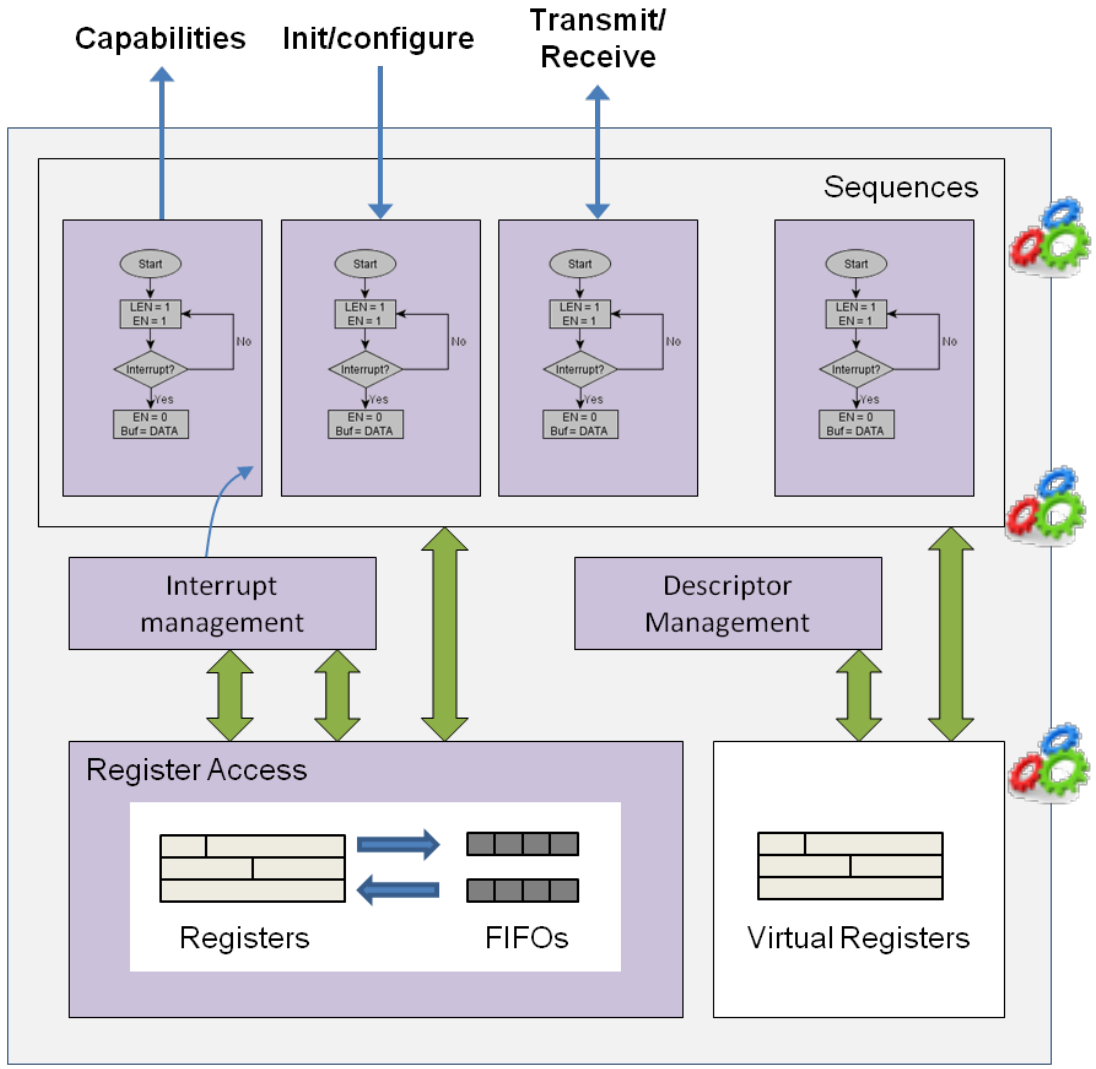
Truly Portable Stimulus Emerging



SYSTEMC SystemVerilog UVM

Test bench

Bare metal drivers for bring up/validation

VxWorks

Firmware/ OS Device Drivers

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Portable Stimulus Example

- TMSC Collaboration Addresses Improved Pattern Generation
  - "Design verification complexity is a major barrier to reach coverage closure. Reducing overall design cycle time is a common goal for the semiconductor industry," said Suk Lee, director of Design Infrastructure Marketing at TSMC. "Our collaboration with Mentor Graphics on Questa Ultra verification platform is an important step to address the time-to-coverage challenges that customers are facing today especially in pattern generation."

- AppliedMicro Sees Dramatic Time-to-Coverage Improvements
  - "AppliedMicro always evaluates tools that make tough design verification challenges easier. The Mentor Graphics collaboration with TSMC results in verification technology that is user friendly and draws on a comprehensive tool set in a standard methodology framework," said Shing Sheung Tse, senior engineering manager at AppliedMicro. "The technology offers the ability to employ advanced techniques and to manage overall coverage metrics for low-power design verification. The Intelligent Testbench Automation capability shortens our time-to-coverage by over 100x. This feature-rich solution helps design teams consolidate tasks, reduce time-to-market and introduce advanced embedded processing for high-speed transport products."

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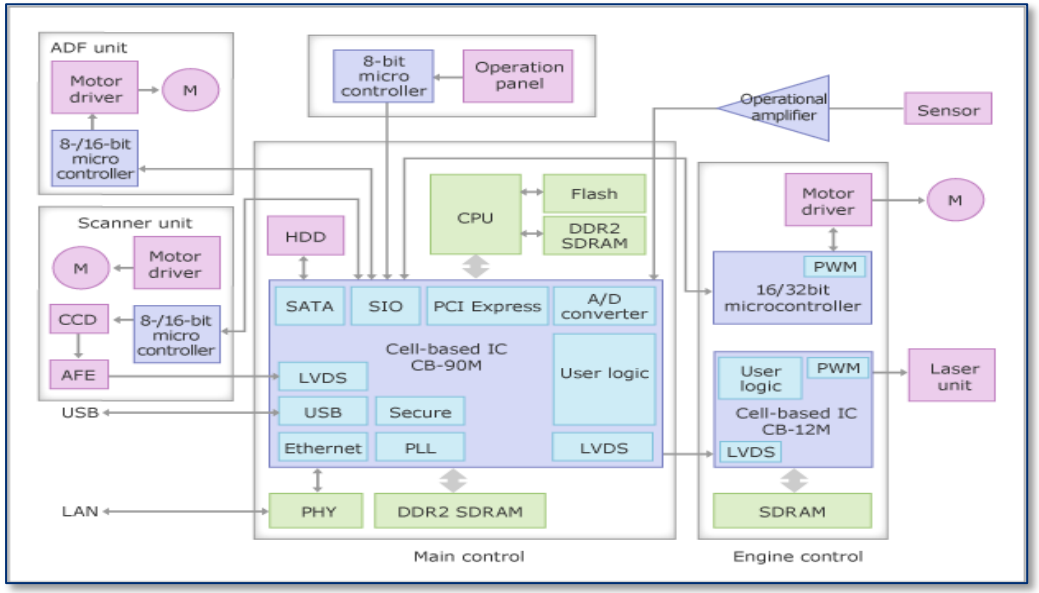
Mentor Portable Stimulus Example

Industry	**Office Products**
Design	**Printer Image Processor**
Existing	**Questa SystemVerilog CRT**

New	**Questa Ultra iTBA**
Value 1	**37 X Faster TTC**
Value 2	**+40% Coverage**
Integration	**½ Day**



Multi-CPU testbench distribution reduced 8 week problem to a 1½ day solution

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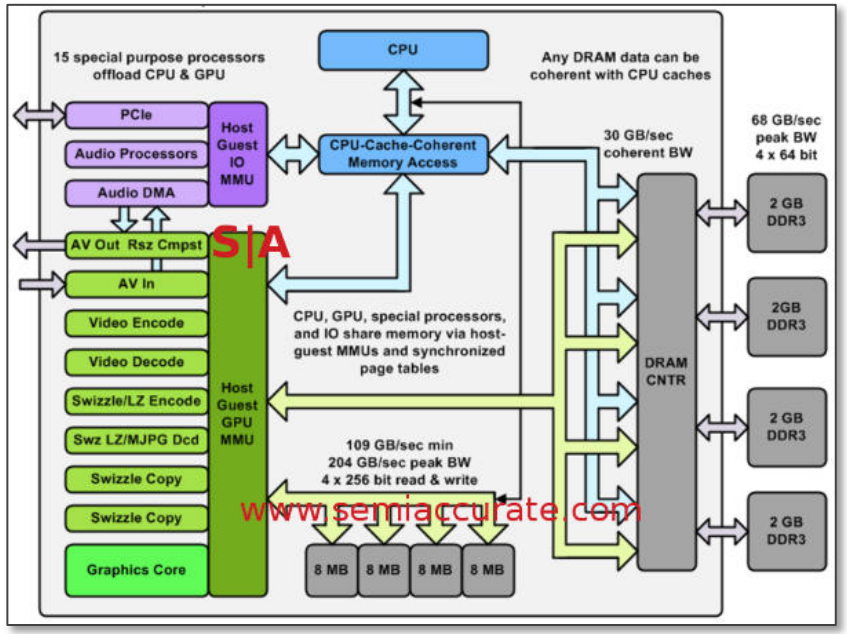
Mentor Portable Stimulus Example

Industry	**Server on Chip**
Design	**Cache Controller**
Existing	**Questa SystemVerilog CRT**

New	**Questa Ultra iTBA**
Value 1	**+90% coverage**
Value 2	**No need to write directed tests**
Integration	**½ Day**



Complex coverage efficiently hit. No need to write directed tests

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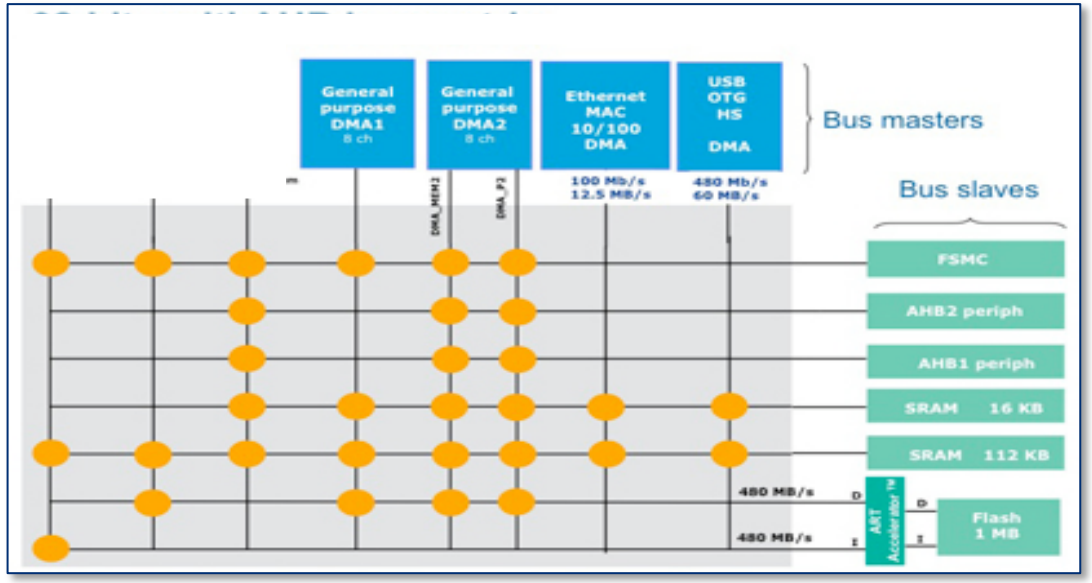
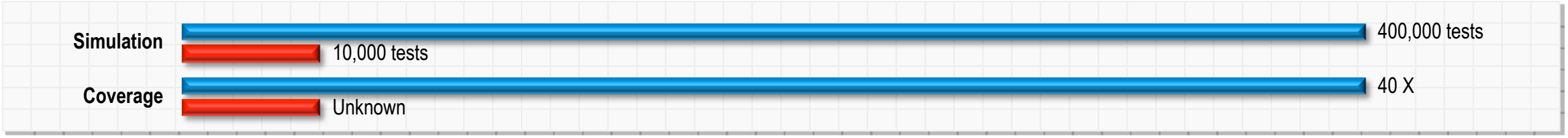
Mentor Portable Stimulus Example

Industry	**Switching Systems**
Design	**Multi-Master Bus Fabric**
Existing	**Questa with directed random tests**

New	**Questa Ultra inFact**
Value 1	**40 X More Tests**
Value 2	**40 X Higher Coverage**
Integration	**2 Days**



Expanded months worth of tests by 40 X in just 2 days. Used inFact to measure coverage.



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Accellera Portable Stimulus Webinar Series

- Part 1: Monday, April 10 at 8:00am PT
  - Discussion of verification productivity
  - Reasons the Portable Stimulus Standard was undertaken
  - Concepts and language constructs
- Part 2: Monday, April 17 at 8:00am PT
  - Block-level stimulus and verification intent models
  - System-level scenarios
  - Generate a test implementation on multiple platforms
- Part 3: Monday, April 24 at 8:00am PT
  - Model coverage
  - Hardware/software interface layer
  - Summary of standardization efforts and upcoming goals.
- Register: Visit http://www.accellera.org/news/events

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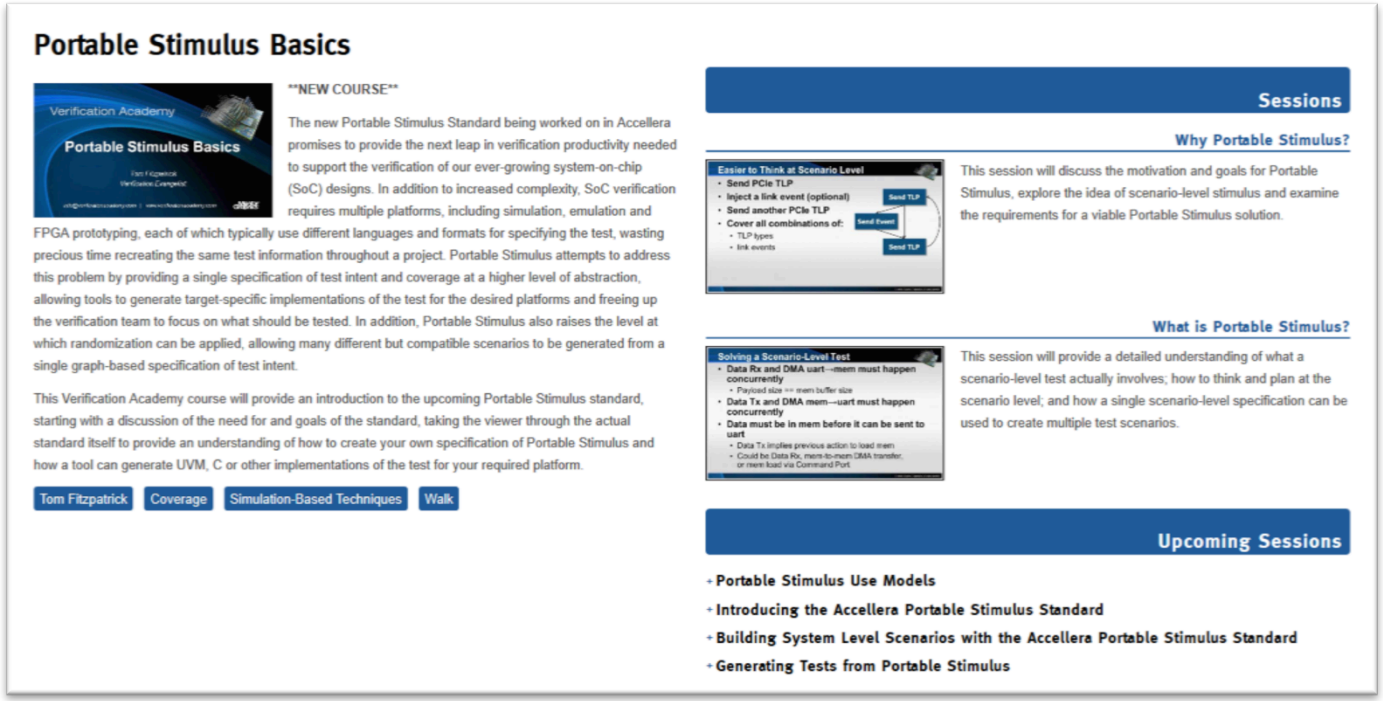
Verification Academy

The most comprehensive resource for verification training

https://verificationacademy.com/courses/portable-stimulus-basics

- Comprehensive on-line training
  - Self-paced training
  - More than 22,000 members
  - New Portable Stimulus course
- World-wide forum discussions
  - 4400+topics
- Verification Methodology
  - Coverage Cookbook
  - UVM Cookbook



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Summary

- Despite design re-use, verification complexity continues to increase at 3-4X the rate of design creation
- Increasing verification requirements drive new capabilities for each type of verification engine
- Continuing verification productivity gains require EDA to:
  - Abstract the verification process from the underlying engines
  - Develop common environments, methodologies and tools
  - Separate the "what" from the "how"
- Portable Stimulus promises another leap in verification productivity
  - Invest in yourself: Keep current with Portable Stimulus development

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