Confidential

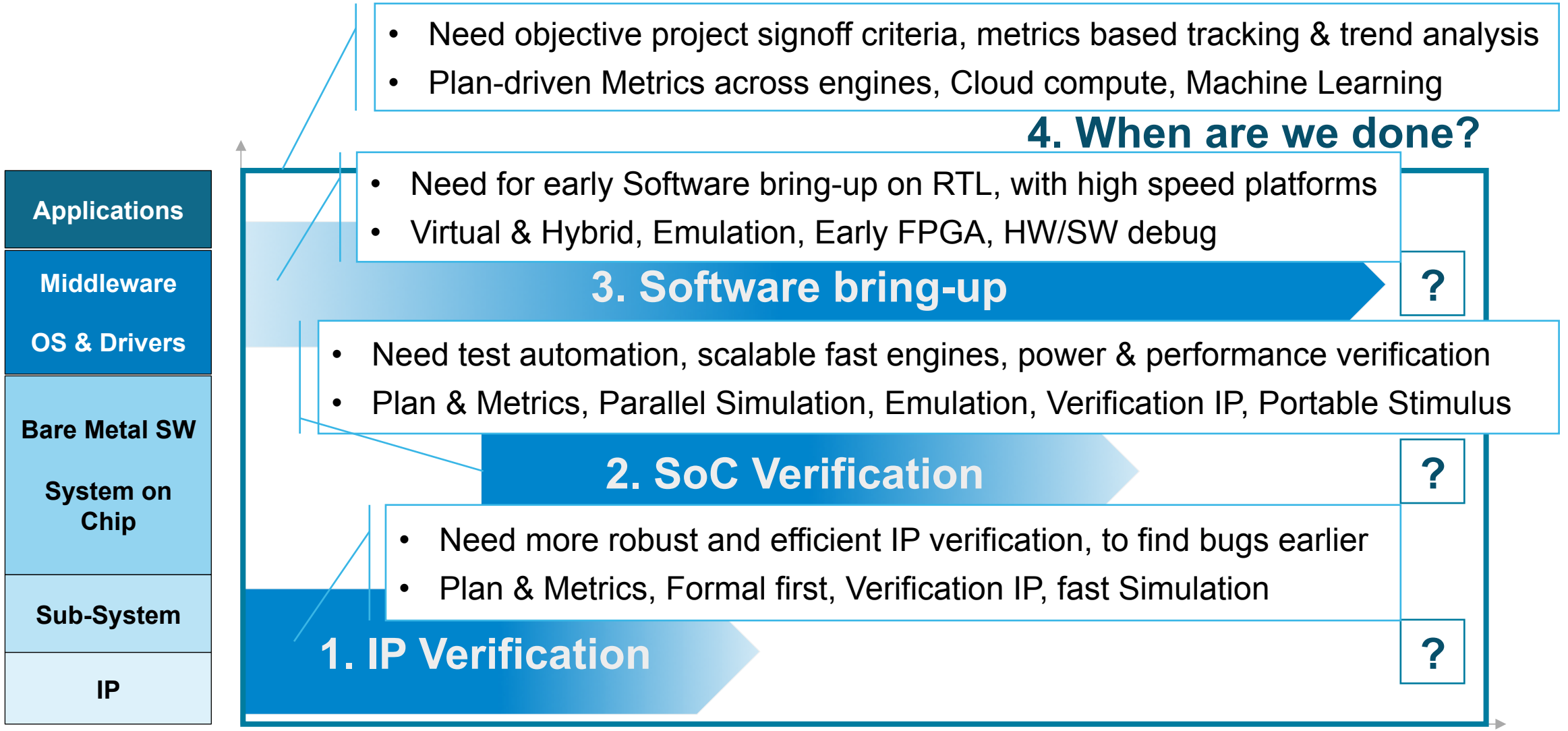
Cadence New Verification Technologies

Accellera Day, Taiwan

April 2017

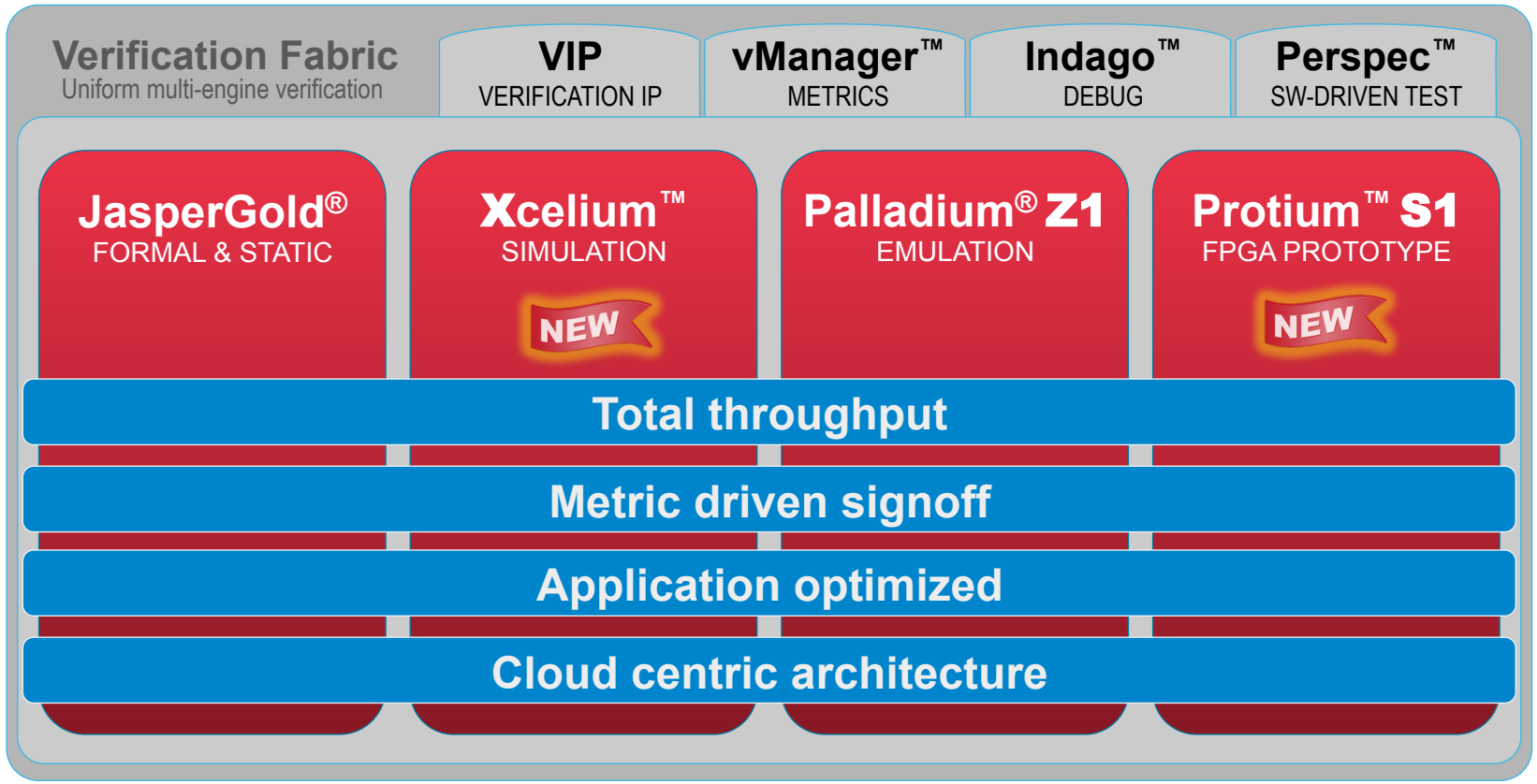
cadence®

Key Verification challenges to address



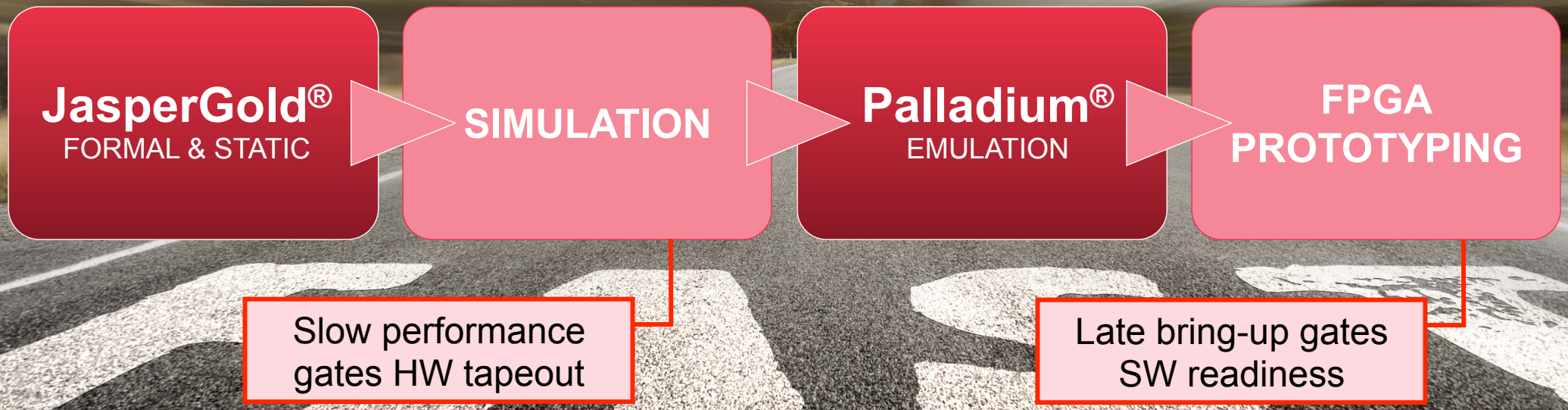
Verification Suite

Technology innovation leadership: *Fast, Smart, and Optimized*



- ***Fast*** **Best-in-class engines**
- ***Smart*** **Flow-driven engine integrations**
- ***Optimized*** **comprehensive solutions**

- **Ever-rising verification** needs driven by growing hardware & software **complexity**
- **Fast time to results** is essential, to ensure projects can **meet schedules**
- **Right tool for the right job:** Formal + Simulation + Emulation + FPGA Prototyping



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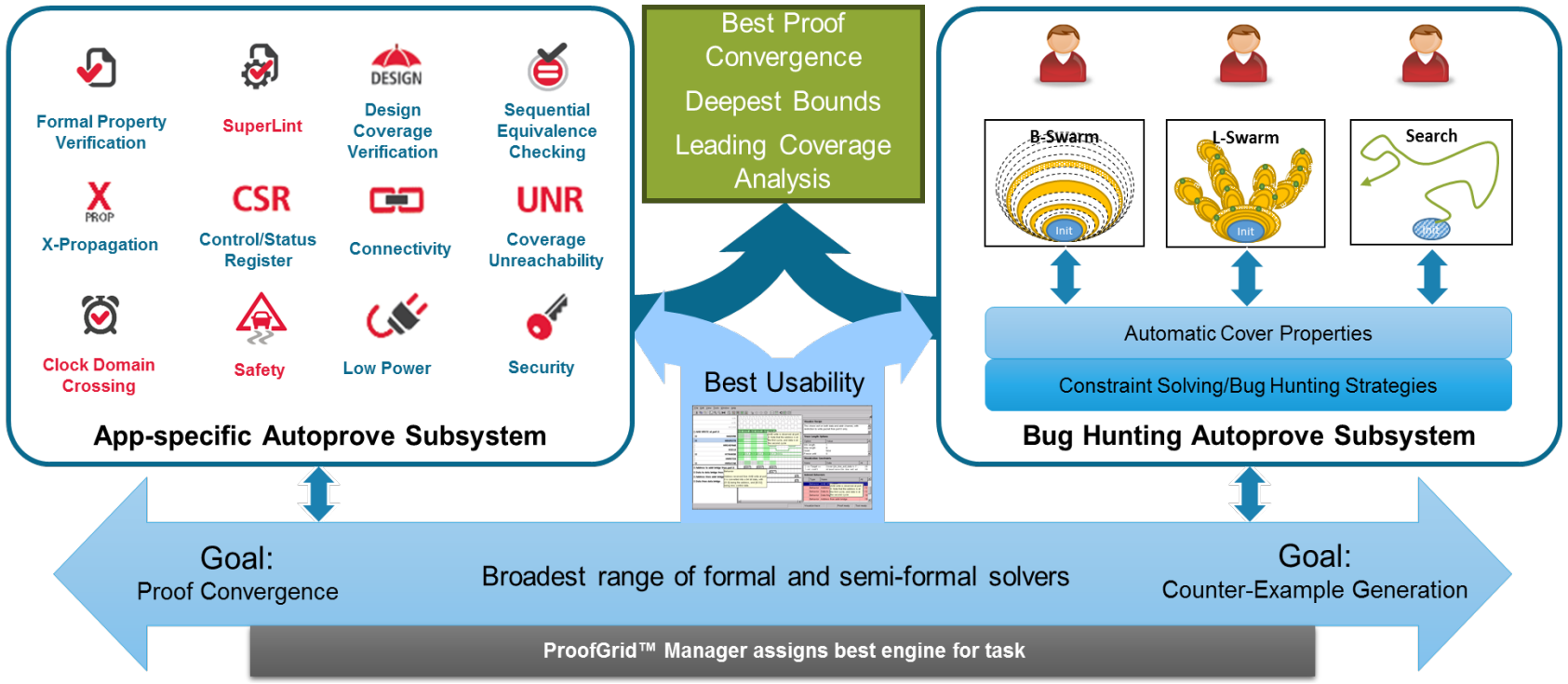
JasperGold – best ease-of-use, capacity and performance

Best engines and subsystems

Targeted and optimized Apps for ease of use

Production use at 9 of top 10 customers



JasperGold formal adoption explosion

17 of the top 20

Top Semiconductor

Companies

Design bring-up benefits

- Another GPU example:
  - Not more, not less bugs, but the bugs are found much earlier
  - So less RTL changes (code churn), especially late

Block	Formal bring-up usage	Bug density total	Code churn total	Bug density late	Code churn late
L2C	High	6	242	1	10
LSC	Medium	8	577	2	34
			460	13	171
			369	4	54
			265	3	53
			254	4	71

Bugs found much earlier: 82% less code churn

2 Jasper User Group Meeting 2013 The Architecture for the Digital World® ARM

*Voted **#1 product in EDA** in 2016*

Source: DeepChip.com

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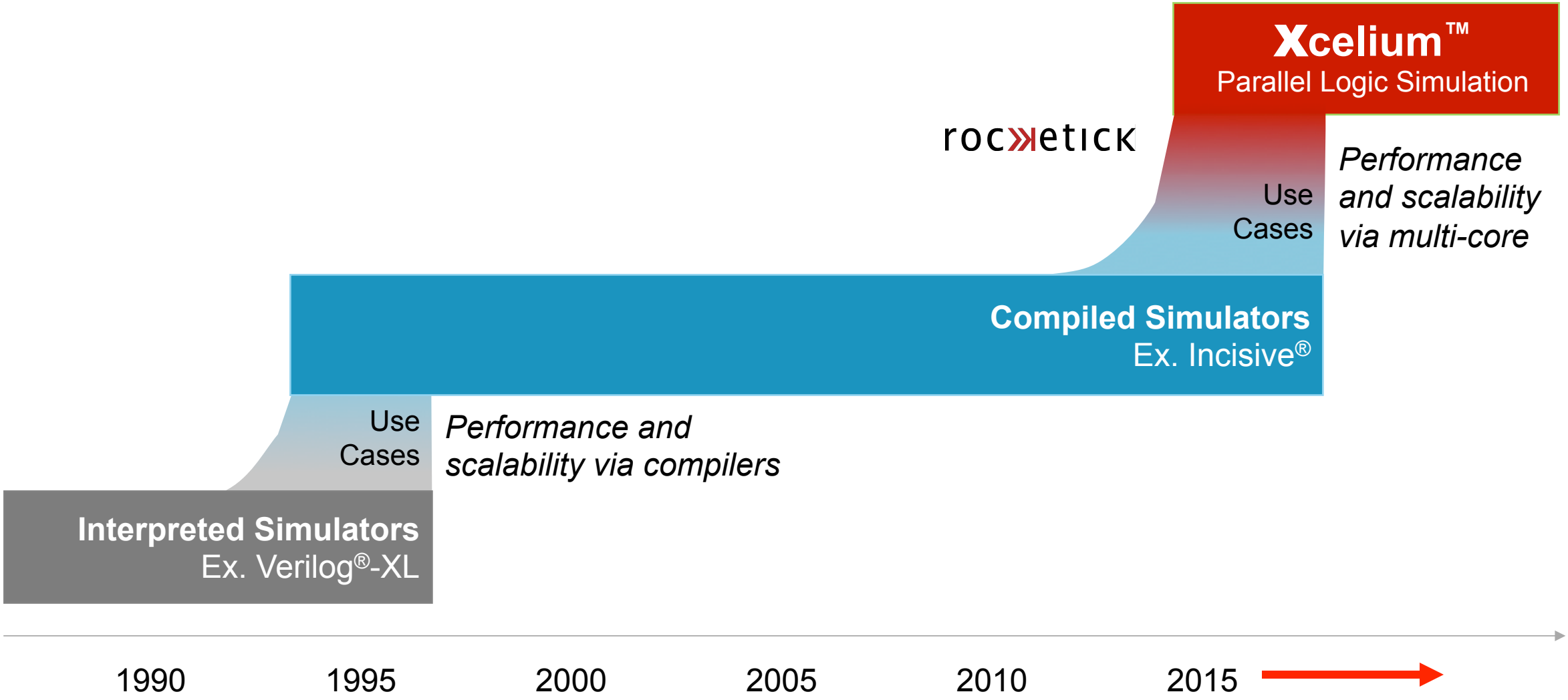
Three generations of simulation

Ushering in the era of parallel simulation



cadence®

New **Xcelium** parallel logic simulation

1st production proven multi-core logic simulation

REVOLUTIONARY

rocketick

PROVEN

Incisive®
Enterprise Simulator

OPTIMIZED

- **2x** avg. single core **speed-up**
- **Direct kernel** engine integration
- **New randomization** engine

- Runs on **standard servers**: 1 to 64 cores
- **Patented** fine-grain multiprocessing technology
- **Top talent** parallel simulation R&D
- In **production use** at market leading companies

Xcelium™

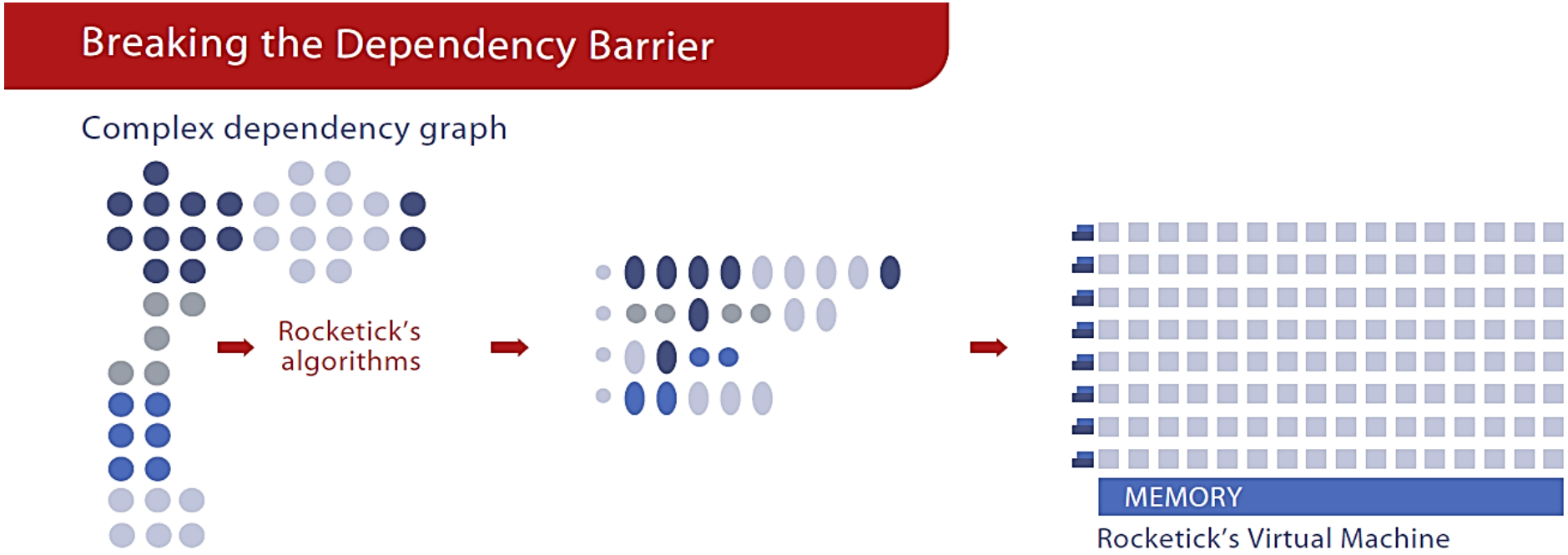
3X+ RTL **5X+** Gate **10X+** DFT

ARM

cadence®

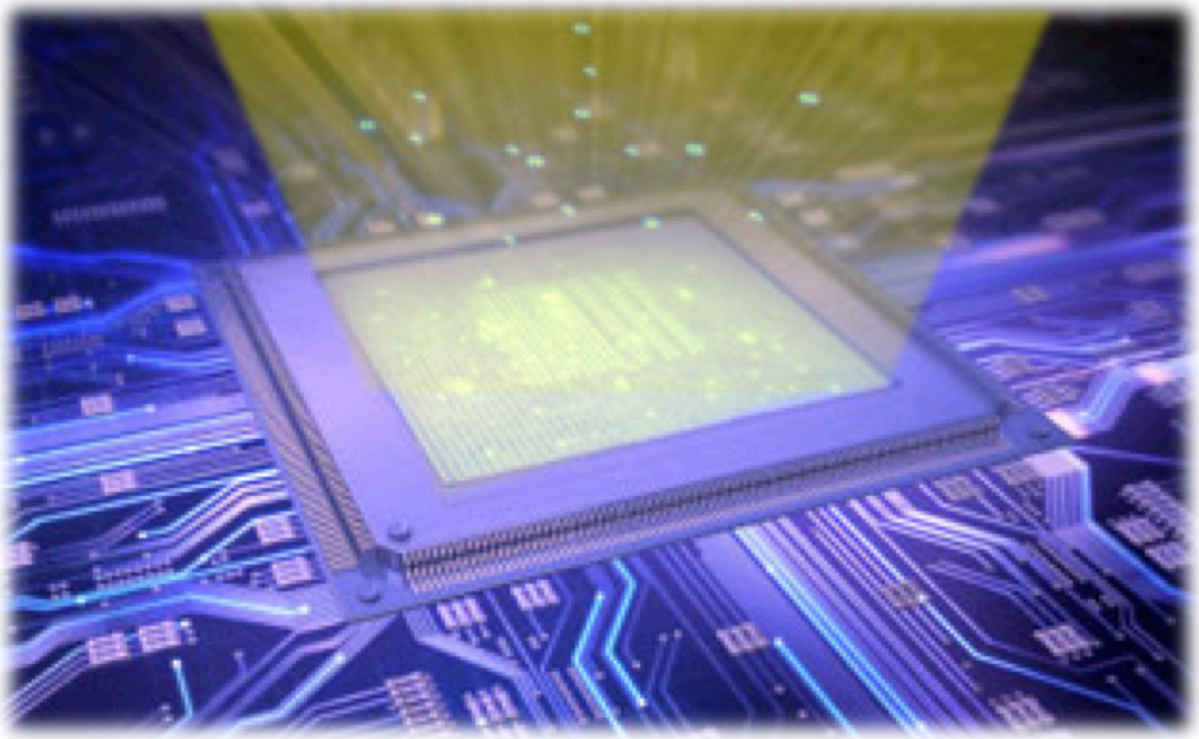
Xcelium contains rocketick Multi-Core technology

Proven core engine for third generation of simulation

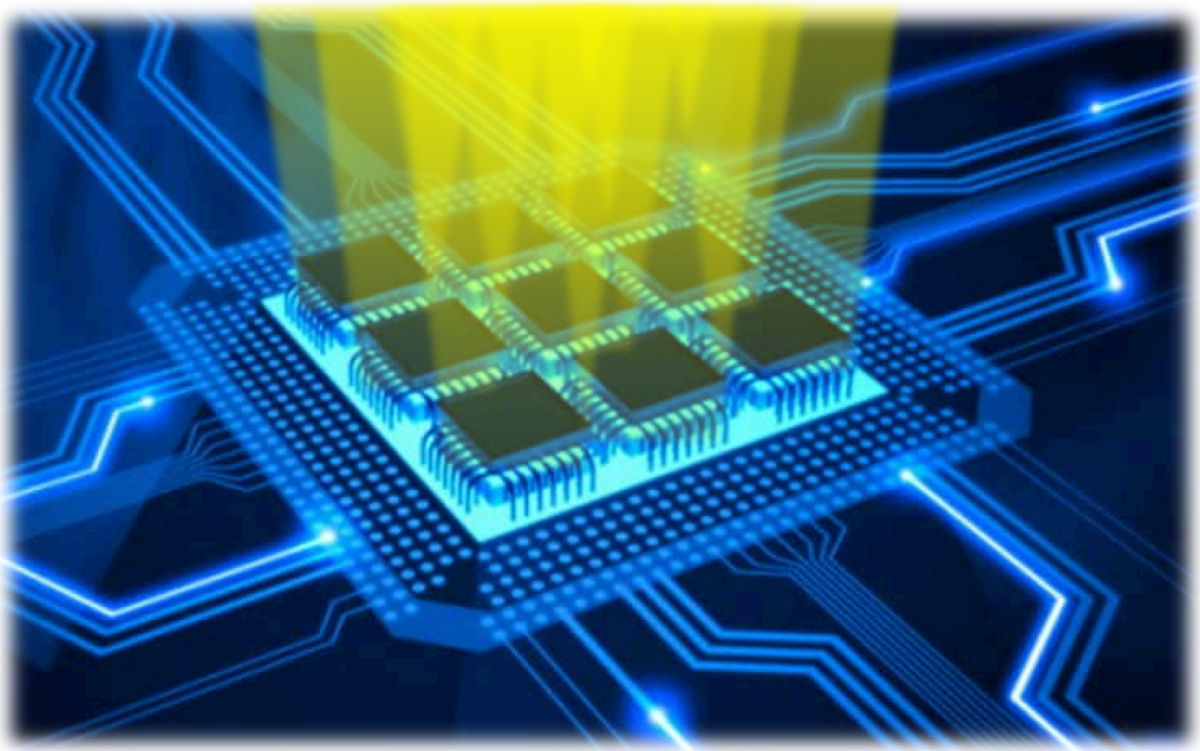


- **Unique** compile/elaboration process analyzes each design's dependency graph
- **Patented** and patent-pending technology, proven scalable beyond a billion gates
- Multi-Core speed-up over Single-Core **performance**

Xcelium performance speed-up



Fast Single-Core performance



Executed leveraging Multi-Core servers

Palladium Z1 emulation

- Palladium® Z1 **enterprise** emulation platform
  - Up to **5X** greater emulation **throughput**
- **Scalability** from IP blocks to full systems on chip
  - Capacity of up to **9.2 billion gates** with **2304 users**
- Best in class **total cost of ownership** (TCO)
  - **22 use models**
- New era of **datacenter-class** emulation
  - **Proven reliability**

16 of the top 20
Top Semiconductor
Companies

9 of the top 10
Top Smartphone / Mobile
Application Processor Suppliers

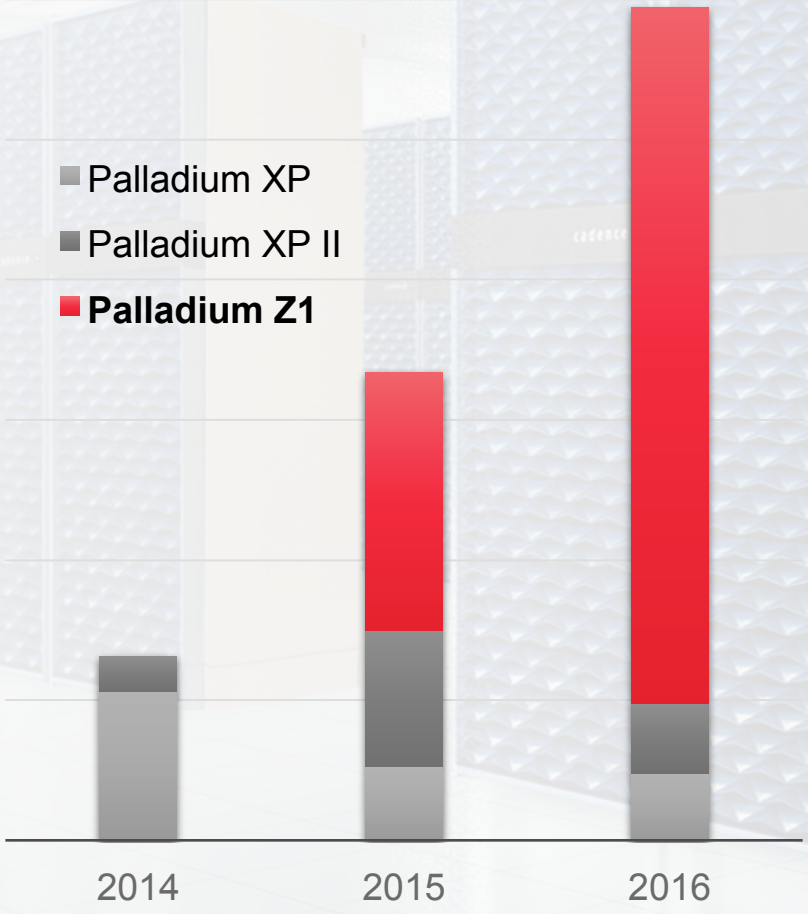
Used in 23 of 25
Top Emulation Consumers

HUAWEI NVIDIA Mellanox TECHNOLOGIES ERICSSON FUJITSU MOBILEYE ARM Imagination CAVIUM

cadence

Palladium Z1 emulation momentum

1.8X annual shipped capacity growth



Palladium® Z1
Versatility
22 Use Models

In-Circuit Emulation
- ❑ ICE with SpeedBridge® adapters
- ❑ ICE with Synthesizable TB
- ❑ Multiuser regressions
- ❖ Emulation Development Kit

Acceleration
- ❑ Simulation Acceleration (SBA, TBA)
- ❑ Code & functional coverage merge
- ❑ In-Circuit Acceleration
- ❑ Gate-level acceleration
- ❑ DFT acceleration
- ❖ Accelerated Verification IP

Virtualization
- ❑ Hybrids with Virtual Platforms
- ❑ Virtual Verification Machine
- ❑ Embedded Testbenches
- ❑ Quick-cycle remote access
- ❖ Emulation Development Kits

Hardware/Software
- ❑ Peripheral software bring-up
- ❑ Hardware and software coverage
- ❑ Software debug
- ❑ Firmware optimization/validation
- ❑ Scenario verification w/ Perspec

Architecture
- ❑ Performance validation / optimization

Post-Silicon
- ❑ ATPG generation
- ❑ Post-silicon validation

Low Power
- ❑ Dynamic Power Analysis w/ Joules™
- ❑ IEEE1801 / UPF / CPF Verification

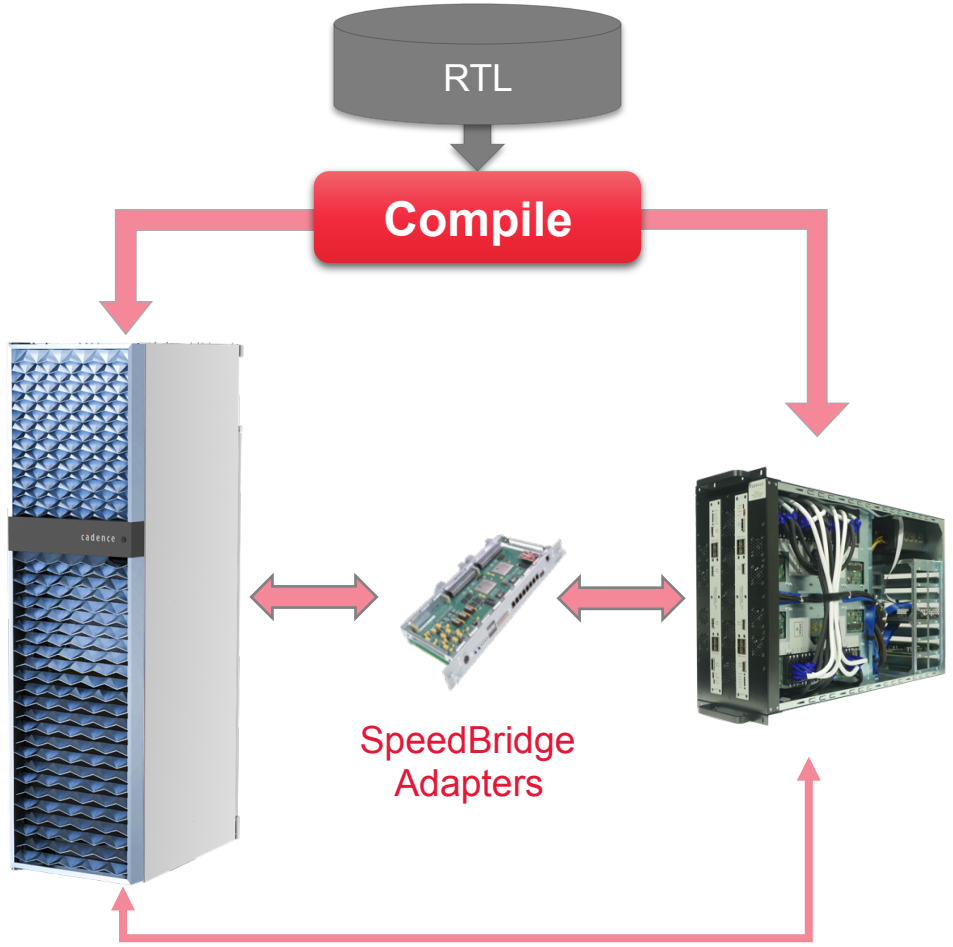
❑ Use Models
❖ Enabling Capabilities

cadence®

Palladium **Z1** + Protium **S1**

Palladium® Z1

- Best debug
- SoC acceleration, HW/SW
- Power & perf. analysis



Protium™ S1

- Highest performance
- SW development
- HW/SW regressions

Congruency and **common environment**

New **Protium S1** FPGA Prototyping

- **Fast bring-up time**: from months to 1-2 weeks
  - No RTL changes | Automatic partitioning | Full FPGA P&R
- **Congruency** with **Palladium® Z1** emulator
  - Common compiler | Environment re-use
- **Scalable performance** (3-100MHz)
  - From fully automatic to user guided | Adv. black-boxing
- Advanced **software debug**
  - Memory upload/download | Force & release | SCE-MI

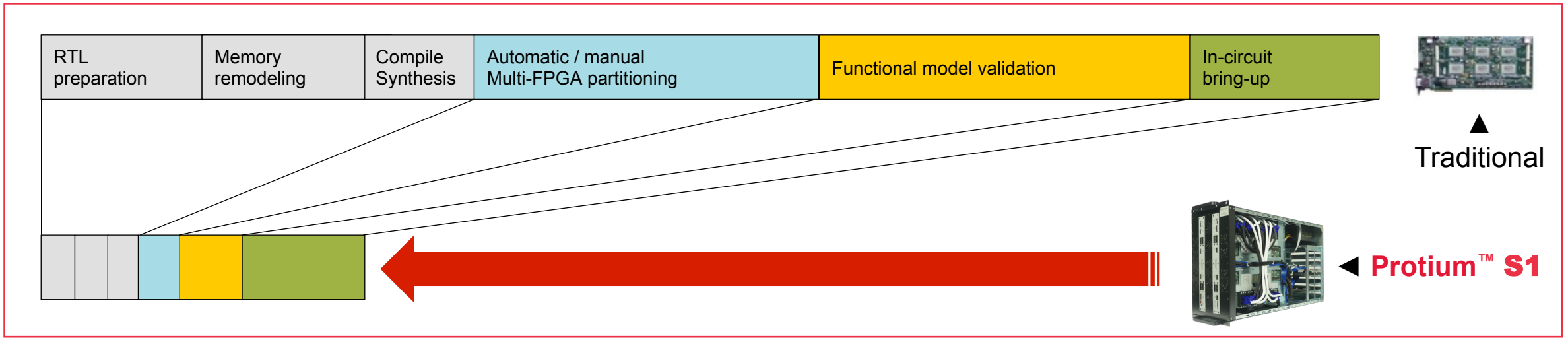
XILINX®

Mellanox® TECHNOLOGIES

cadence®

Protium S1 enables fast prototype bring-up

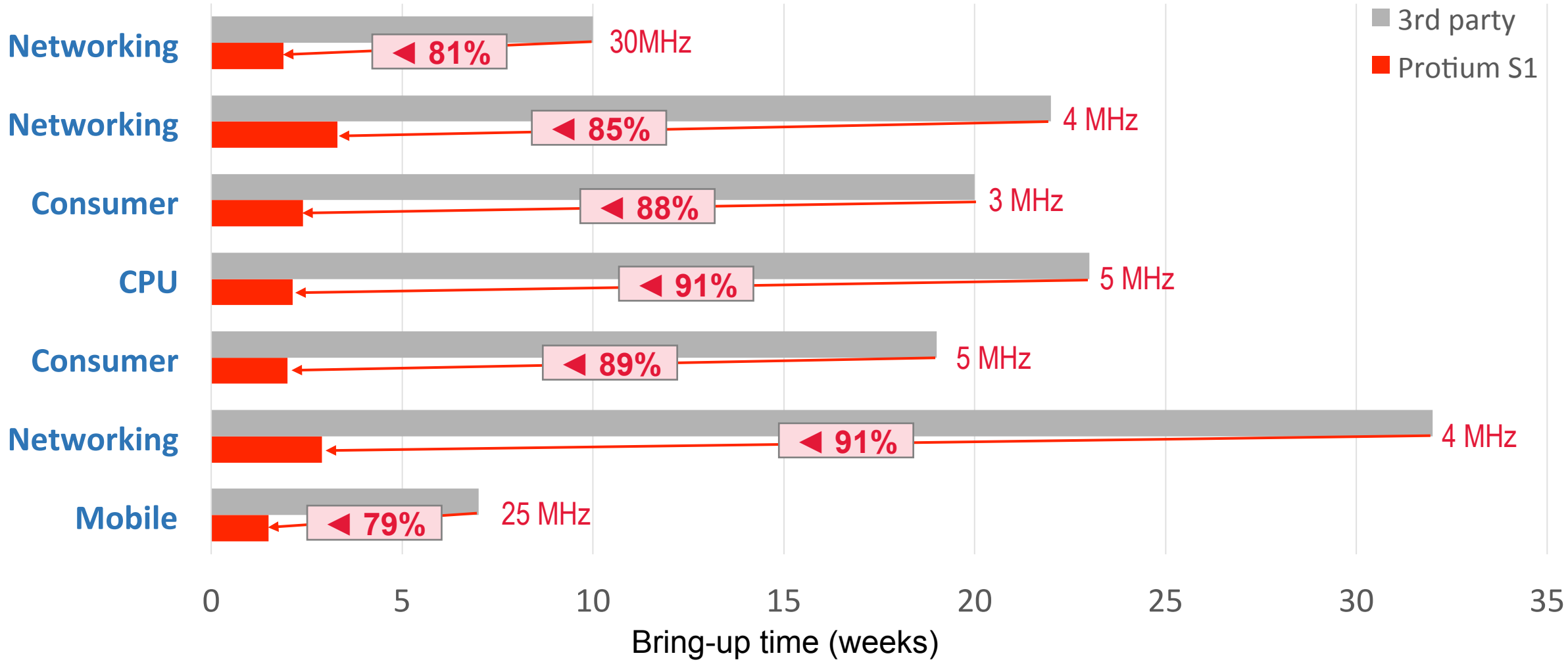
Reducing time-to-prototype (TTP) from months to weeks



- No RTL modifications needed
  - Clocking / number of clocks
  - Automated memory compilation and modeling
- Fully automatic, multi-FPGA partitioning
  - Optional manual optimization
- Pre-FPGA P&R model validation
  - Multiple design integrations per day
  - Avoids time-consuming FPGA P&R
- Fully integrated FPGA P&R
  - Automatic constraint generation
  - Guaranteed P&R success

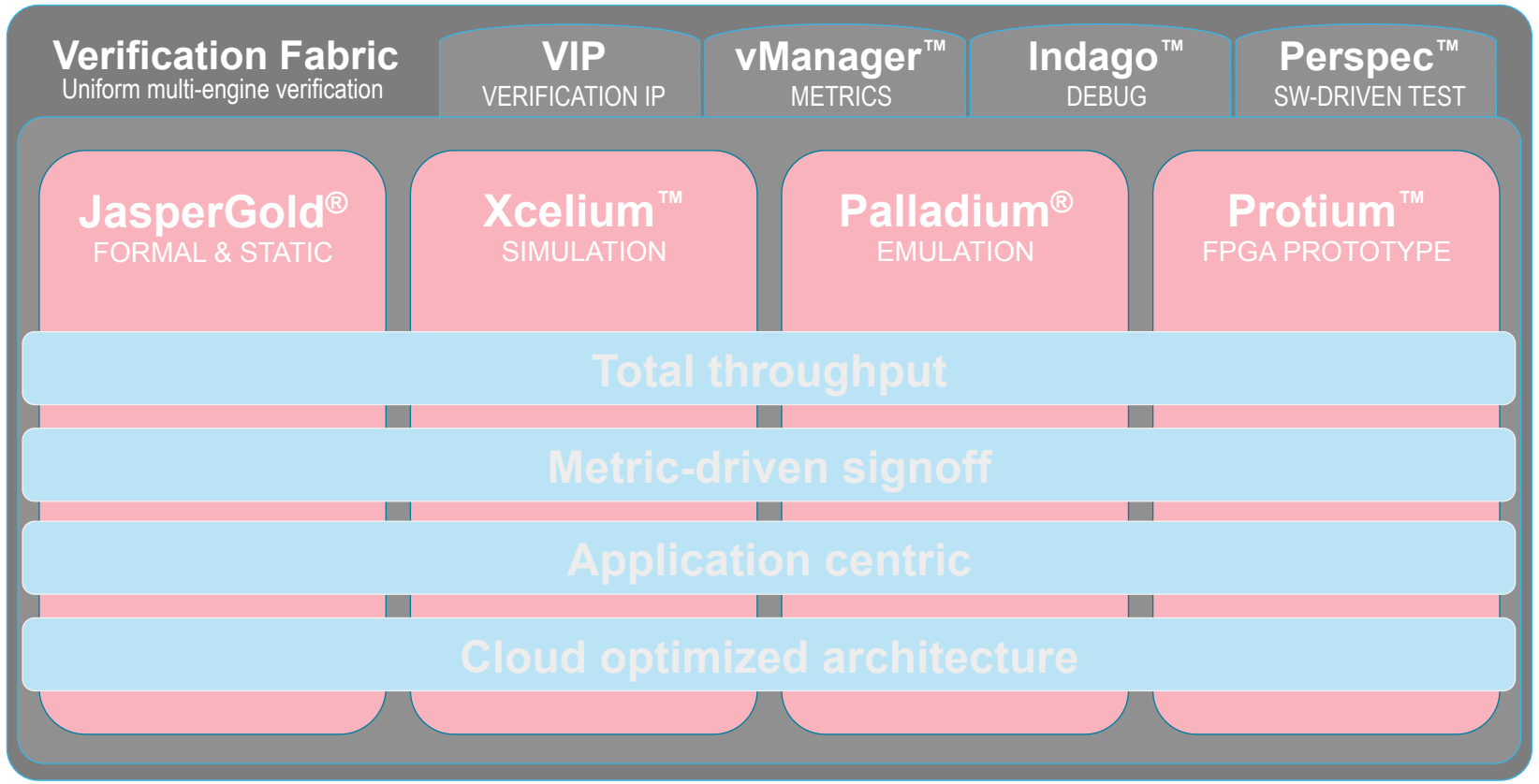
Protium S1 faster bring-up time and initial performance

Customer examples



Verification Suite – Verification Fabric

Technology innovation leadership: *Fast, Smart, and Optimized*



- ***Fast*** **Best-in-class engines**
- ***Smart*** **Flow-driven engine integrations**
- ***Optimized*** **comprehensive solutions**

Verification fabric

Multi-engine verification environment automation

- Unique multi-user plan management
- Industry-leading VIP titles and use
- Comprehensive debug
- Innovative source-independent test generation

Perspec™ System Verifier → SOC

UVM → IP

1st

Drive

Plan

JasperGold® FORMAL & STATIC

Xcelium® SIMULATION

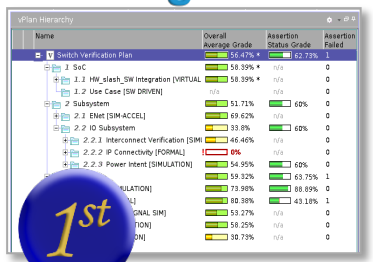
Palladium® EMULATION

Protium™ FPGA

Analyze

Construct

vManager™ Platform

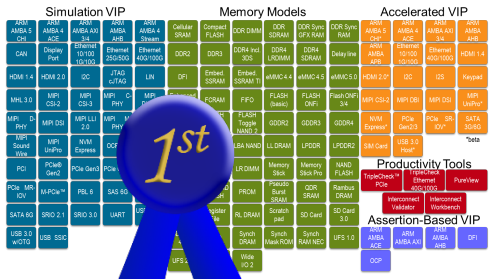


1st

vManager™ Platform

1st

VIP Catalog



1st

Verification IP

Protocol I/F + Memory Models

Virtual / SpeedBridge® Adapters

SoC Workbench

Indago™ Debug Platform

- Strong TB & ESW debug
- Adding new debug apps

cadence

Expanding **Verification IP** portfolio leadership, with latest titles

Simulation VIP

ARM AMBA 5 CHI	ARM AMBA 4 ACE	ARM AMBA AXI 3/4	ARM AMBA AHB	ARM AMBA 4 Stream
CAN	Display Port	Ethernet 10/100 1G/ 10G	Ethernet 25G/50G	Ethernet 400G/200G
Ethernet TSN	HDMI 1.4/2.0	I2C	JTAG cJTAG	LIN
MHL 3.0	MIPI CSI-2	MIPI CSI-3	MIPI C-PHY	MIPI DigRF
MIPI I3C	MIPI DSI incl. DBI, DPI	MIPI DSI2 incl. DBI, DPI	MIPI LLI 2.0	MIPI M-PHY
MIPI SLIMbus	MIPI Sound Wire	MIPI UniPro	NVM Express	OCP 2.2
OCP 3.0	PCI	PCIe Gen2	PCIe Gen3	PCIe Gen4
PCIe SR-IOV	PCIe MR-IOV	M-PCIe	PLB 6	SAS 6G
SAS 12G	SATA 24G	SRIO 2.1	SRIO 3.0	UART
USB 2.0 w/ OTG	USB 3.0 w/ OTG	USB 3.1 w/ OTG	USB Type-C/PD	Wireless 802.11 MAC
Bluetooth LE	CCIX			

Memory Models

Cellular SRAM	Compact FLASH	DDR DIMM	DDR SDRAM	DDR Sync GFX RAM	DDR Sync RAM
DDR2	DDR3	DDR4 Incl. 3DS	DDR4 LRDIMM	DDR4 SDRAM	Delay line
DFI	Embed. SSRAM	Embed. SSRAM TI	eMMC 4.4	eMMC 4.5	eMMC 5.0
Enhanced SDRAM	FCRAM	FIFO	FLASH (basic)	FLASH ONFi	Flash ONFi 3/4
FLASH PPN DDR	FLASH Toggle NAND	FLASH Toggle NAND 2	GDDR2	GDDR3	GDDR4
HBM	HMC	LBA NAND	LL DRAM	LPDDR	LPDDR2
LPDDR3	LPDDR4	LR DIMM	Memory Stick	Memory Stick Pro	NAND FLASH
NOR FLASH Spansion	One NAND FLASH	PROM	Pseudo Burst SRAM	QDR SRAM	Rambus DRAM
Rambus Turbo Mode	Register File	RL DRAM	Scratch pad	SD Card	SD Card 3.0
SD Card 4.0	SDIO	Synch DRAM	Synch Mask ROM	Synch RAM NEC	UFS 1.0
UFS 2.1	Wide I/O	Wide I/O 2	LPDDR5	DDR5	Octal SPI
UFS 2.1	HyperFlash	NVDIMM-P			

Accelerated VIP

ARM AMBA 5 CHI*	ARM AMBA 4 ACE	ARM AMBA AXI 3/4	ARM AMBA AHB
ARM AMBA APB	Ethernet 10/100 1G/ 10G	Ethernet 25G/50G*	Ethernet 40G/100G
HDMI 1.4	HDMI 2.0*	I2C	I2S
Keypad	MIPI CSI-2	MIPI DBI	MIPI DSI
MIPI UniPro*	NVM Express*	PCIe Gen2/3	PCIe SR-IOV*
SATA 3G/ 6G Device	SIM Card	USB 2.0 w/ OTG*	USB 3.0 Host*

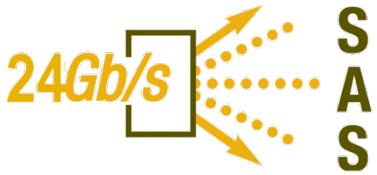
Productivity Tools

PureView	Indago Protocol Debug App	Interconnect Workbench	Interconnect Validator
TripleCheck PCI Express	**TripleCheck** MIPI CSI-2	TripleCheck MIPI UniPro	TripleCheck MIPI SoundWire
TripleCheck BLE	TripleCheck WiFi		

Assertion-Based VIP

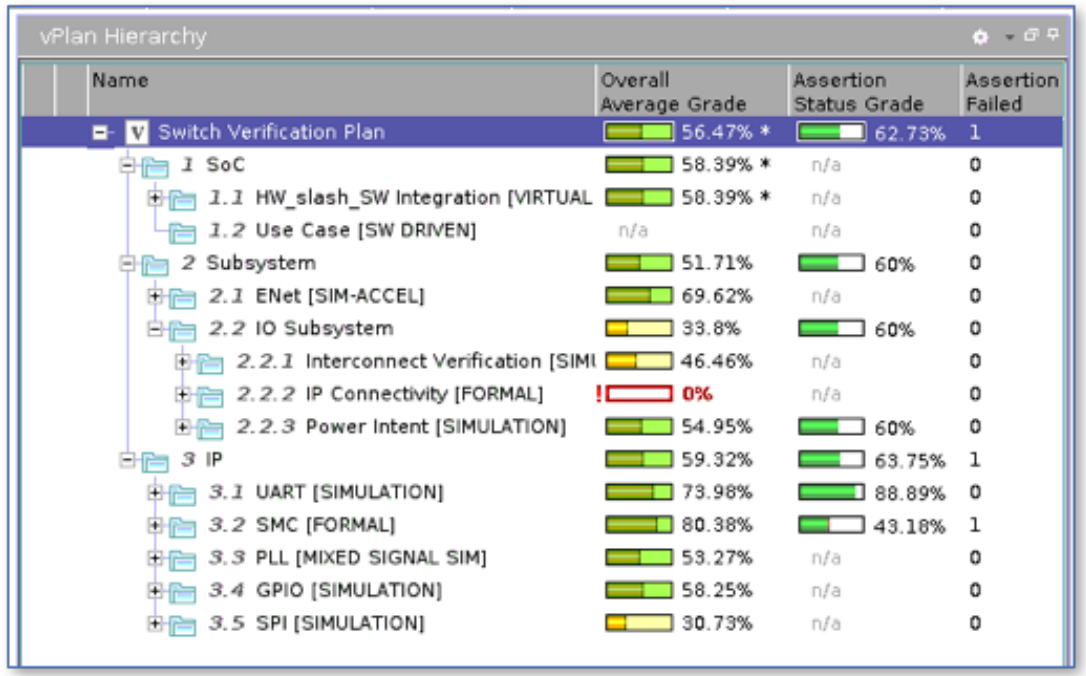
ARM AMBA ACE	ARM AMBA AXI	ARM AMBA AHB	DFI
OCP			

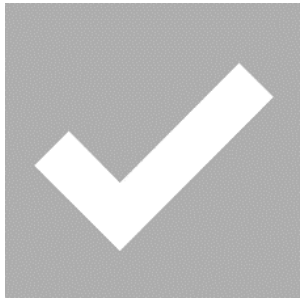
Recent and upcoming **VIP**s



DDR5 **HyperFlash** **LPDDR5** NVDIMM-P **Octal SPI**

Plan-driven multi-engine verification metrics with **vManager**





JasperGold

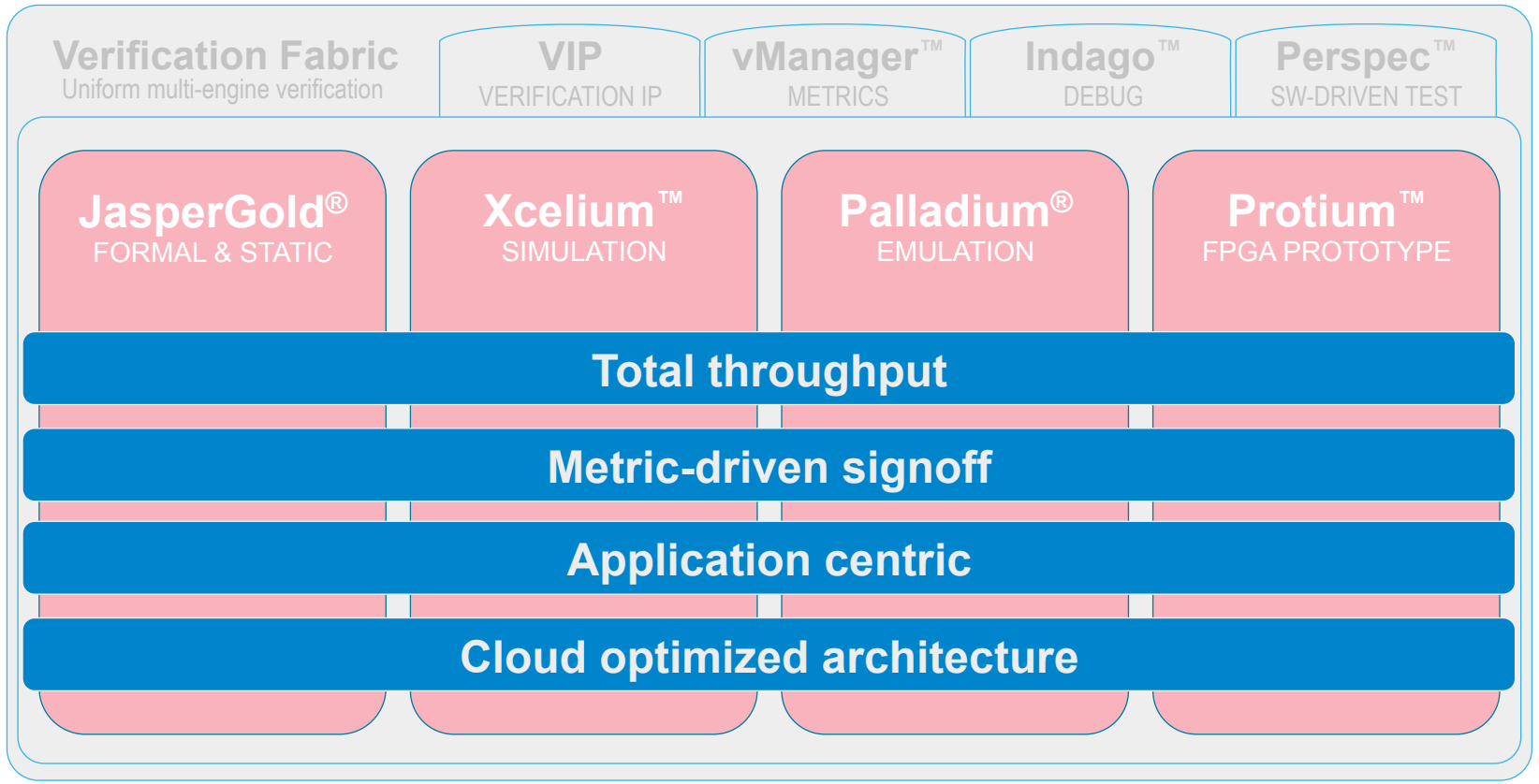
Verification IP

Xcelium

Palladium

Verification Suite – Solutions

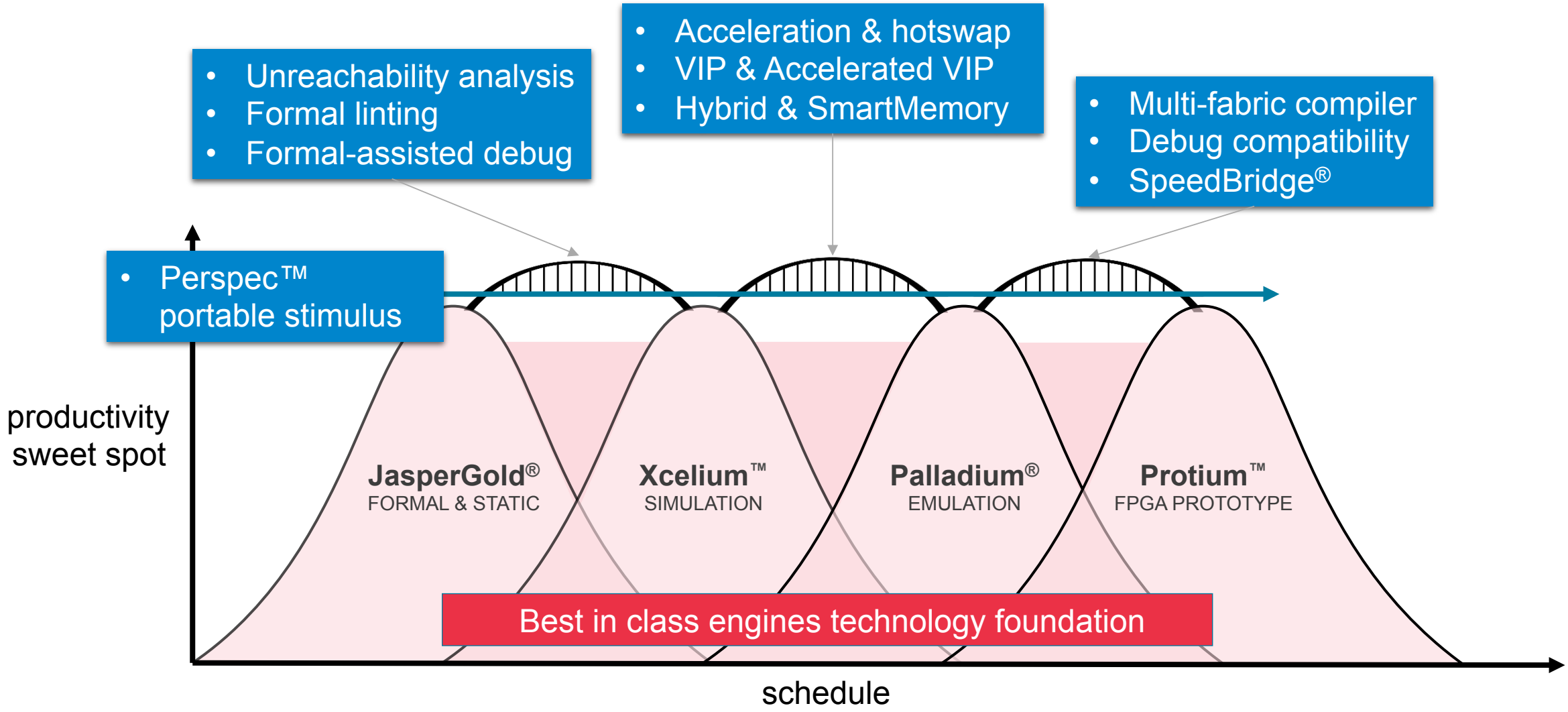
Technology innovation leadership: *Fast, Smart, and Optimized*



- ***Fast*** **Best-in-class engines**
- ***Smart*** **Flow-driven engine integrations**
- ***Optimized*** **comprehensive solutions**

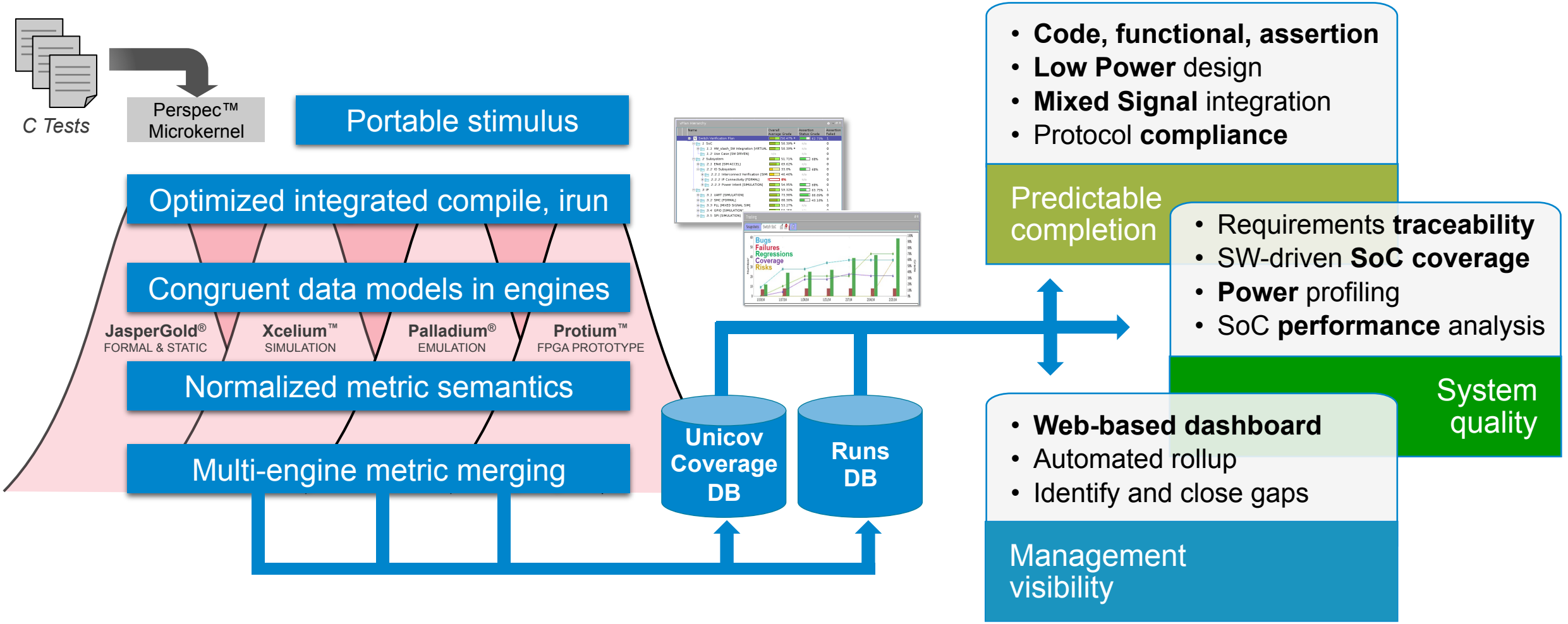
Total throughput

Schedule and turn-around-time reduction

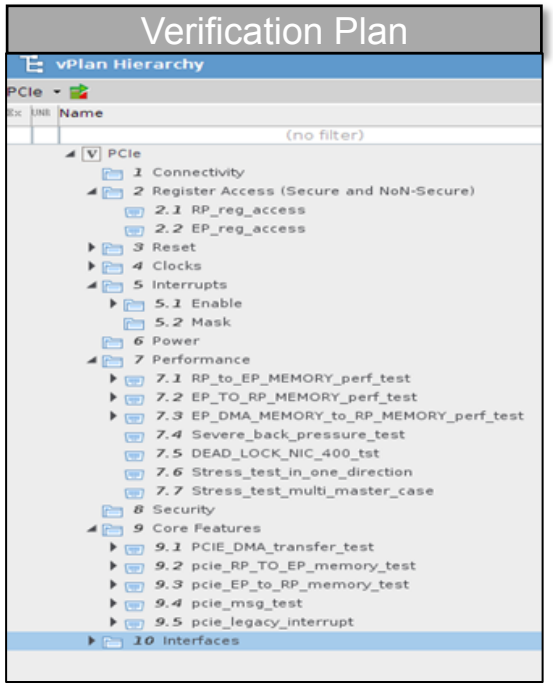


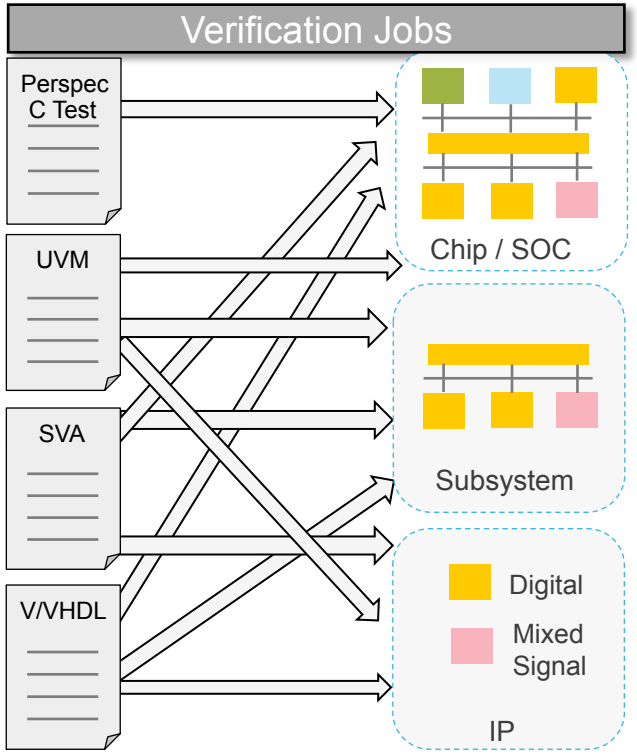
Metric-driven signoff

Quality via multi-engine metrics aggregated in vManager, IP to SoC level



Functional signoff with requirements traceability, dashboards

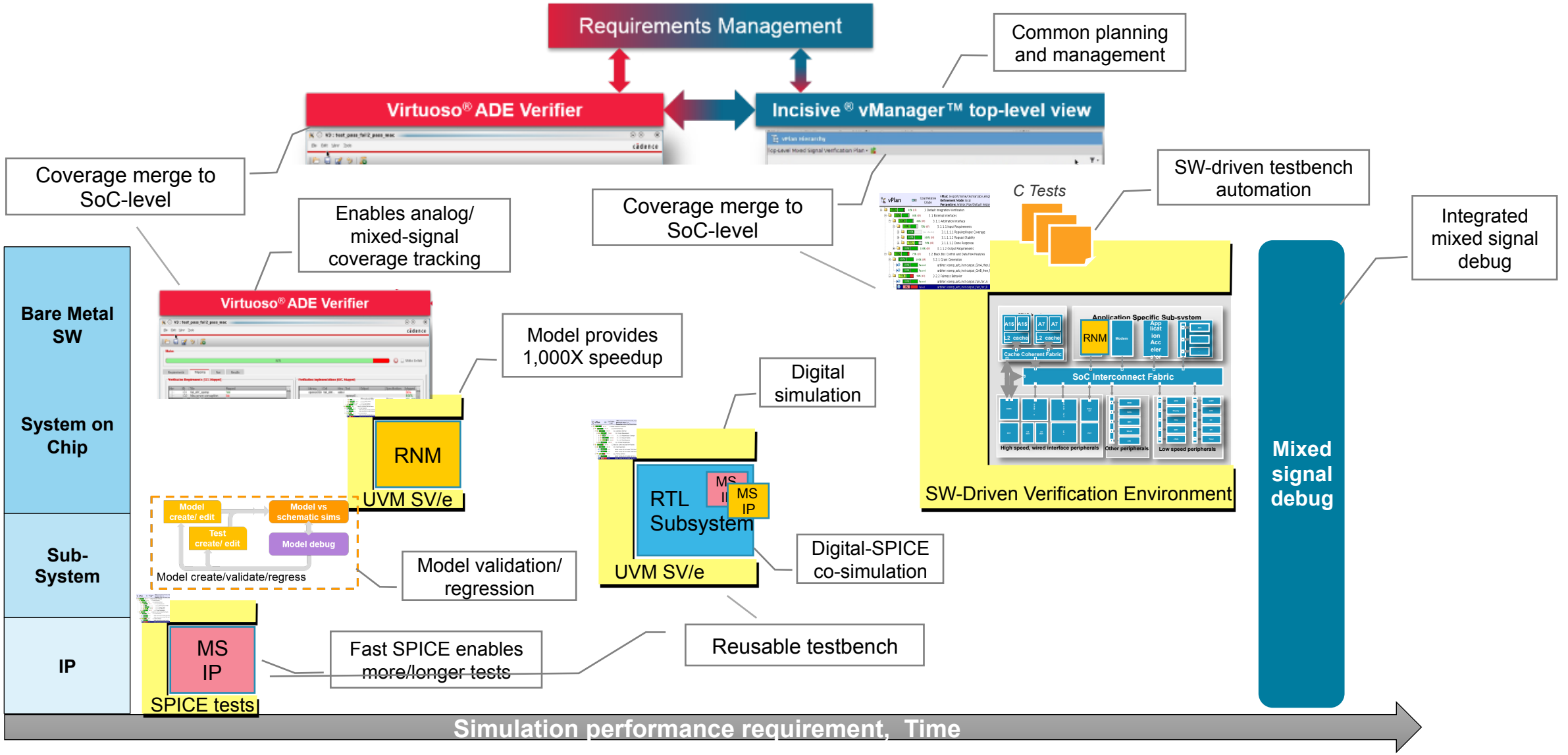




Defines ‘What’ to Verify
Defines Sign-Off Criteria

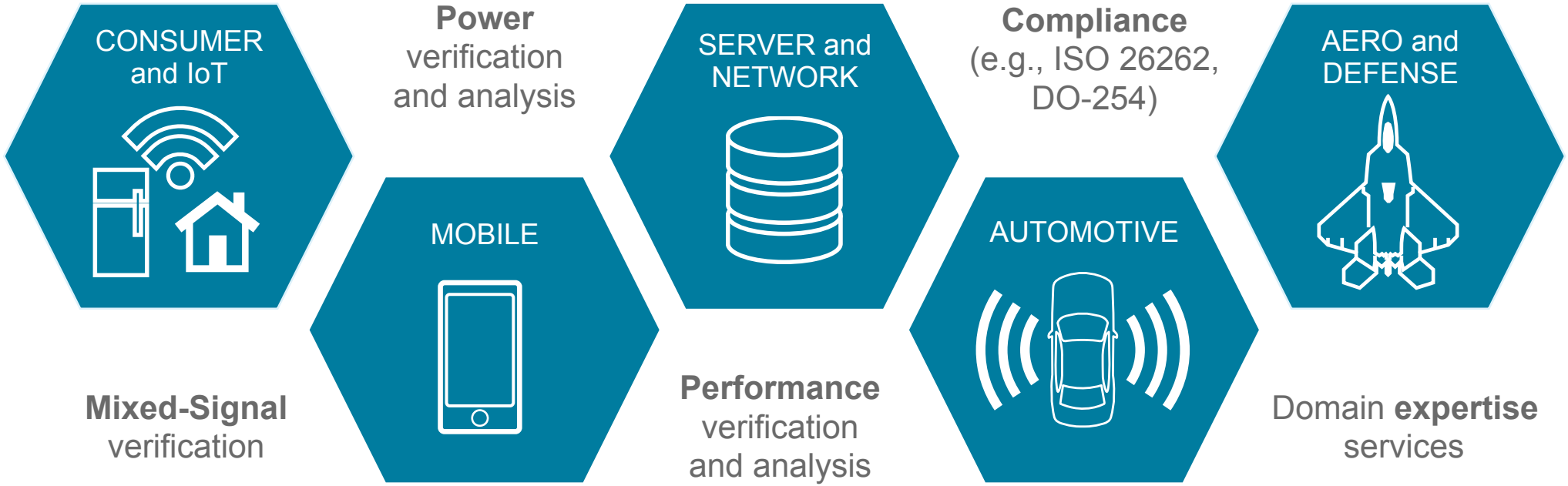
JasperGold®	Xcelium™	Palladium® Z1	Protium™ S1
FORMAL	SIMULATION	EMULATION	FPGA PROTO

Mixed-signal verification signoff



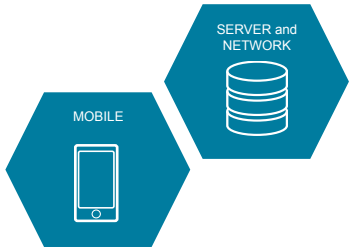
Application centric

Vertical-tailored IP to SoC to HW/SW co-verification and SW bring-up



Distinct vertical applications bring additional verification requirements

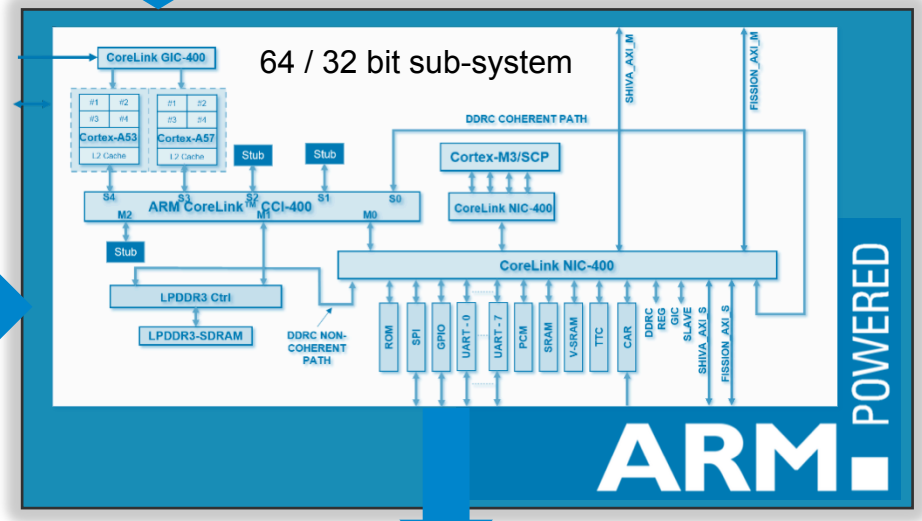
ARM-based flow for Mobile and Server

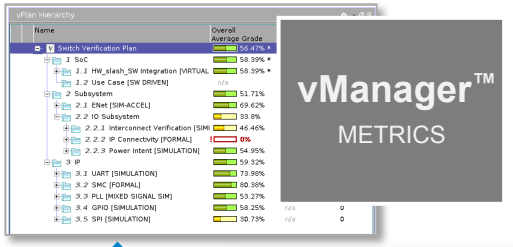


Perspec™
SW-DRIVEN TEST

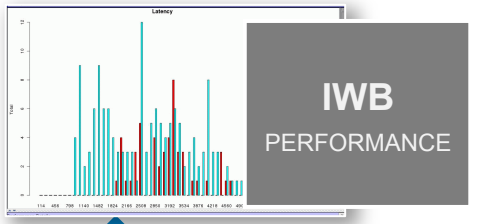
C Tests

VIP

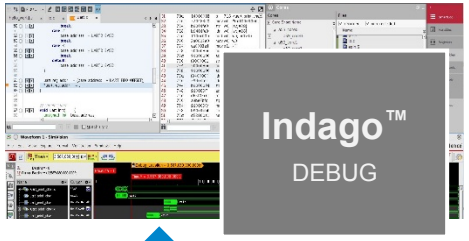




vManager™
METRICS



IWB
PERFORMANCE



Indago™
DEBUG

JasperGold®
FORMAL

Xcelium™
SIMULATION

Palladium® Z1
EMULATION

Protium™ S1
FPGA PROTO

2 - 10X+
Faster simulation

1 MHz
3 day bring-up from Xcelium

11.9 MHz
4 day bring-up from Palladium

Unicov Coverage DB

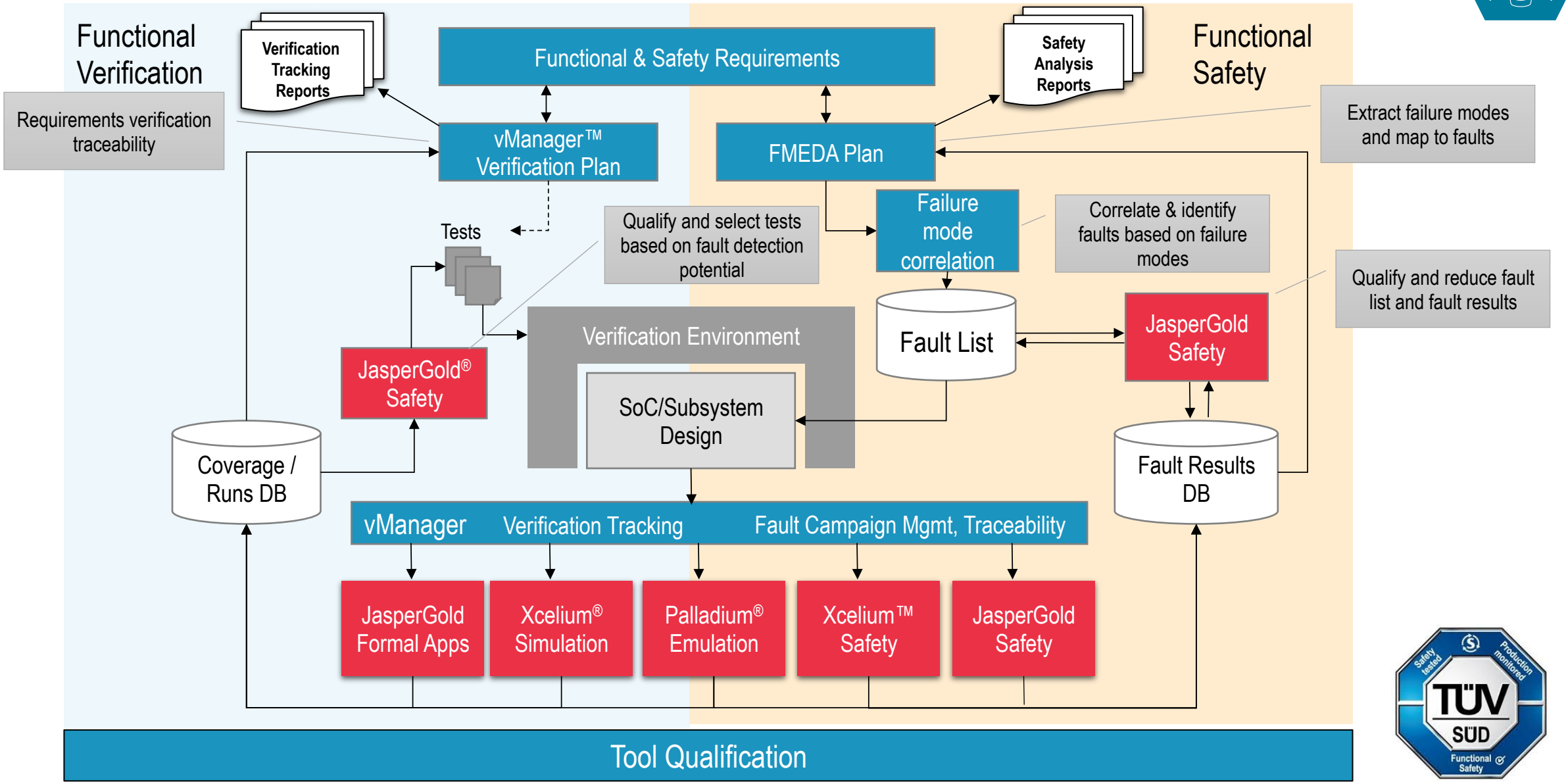
Runs DB

Debug DB

CADENCE CONFIDENTIAL

cadence®

Cadence safety verification flow view



End-to-end efficiency and productivity with full **Verification Suite**

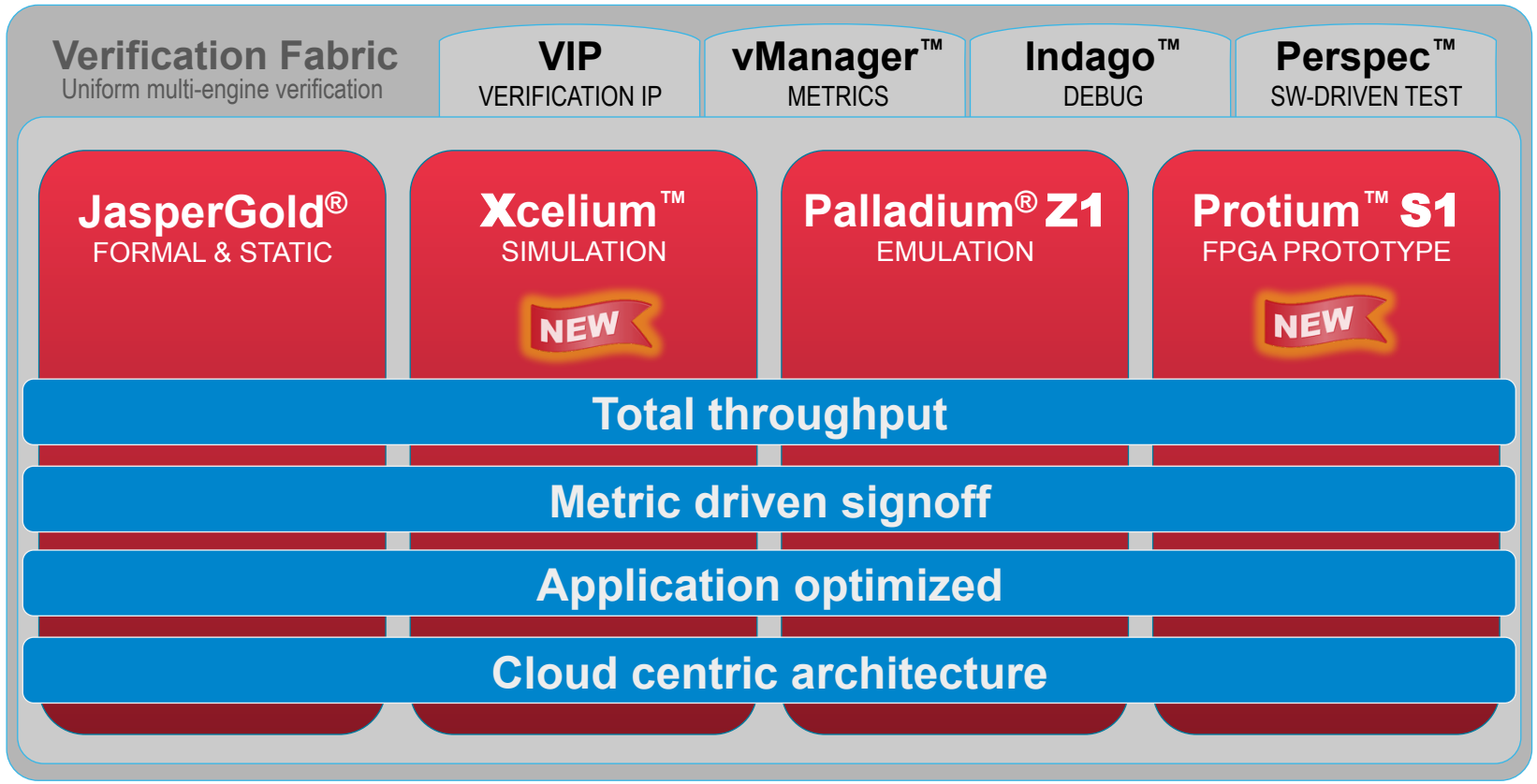
Prime vendor consolidation at large European Telecom OEM

- Challenge: inefficient system design & verification
  - Shrinking project schedules, TAT
  - Rise in SoC complexity
  - Lack of horizontal flow reuse
  - Multi-vendor inefficiency, cost
  - Growing early SW and HW/SW issues

- Solution
  - Consolidation with Cadence for delivery of complete verification flow
    - Xcelium™ platform as verification framework glue
    - Adoption and scaling of Palladium® Z1 usage for HW and HW/SW
    - Expansion in use of JasperGold® and Verification IP
  - Close collaboration on upgrades from MENT & SNPS technologies to CDNS
  - Flow driven partnership with new technology use: Perspec™, Indago™, …

Verification Suite

Technology innovation leadership: *Fast, Smart, and Optimized*



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